Dr. MAHALINGAM
COLLEGE OF ENGINEERING AND TECHNOLOGY
Udumalai Road, Pollachi, Coimbatore District - 642003
Established in 1998 ♦ Approved by AICTE ♦ Affiliated to Anna University
(A DIVISION OF NIA EDUCATIONAL INSTITUTIONS)
An Autonomous Institution
Since 2011
NAAC A++ GRADE
Cycle 3 (2023-2030)
The Highest Grade

Curriculum and Syllabi

Semesters I to VIII

Regulations 2023

(2024 Batch onwards)

Dr. Mahalingam College of Engineering and Technology, Pollachi 642003.

(An autonomous institution approved by AICTE and affiliated to Anna University)

Department of Electronics Engineering (VLSI Design and Technology)

VISSION

- To strive for excellence in Electronics and Semiconductor Engineering education, research and technological services imparting quality training to students, to make them competent and motivated engineers.

MISSION

- Impart high quality technical education in Electronics and Semiconductor Engineering through effective teaching- learning process and updated curriculum.
- Equip the students with professionalism and technical expertise to provide appropriate solutions to societal and industrial needs.
- Provide stimulating environment for continuously updated facilities to pursue research through creative thinking and team work.

Programme Educational Objectives (PEOs) – Regulations 2023

B.E. Electronics Engineering (VLSI Design and Technology) graduates will:

PEO1. Technical Expertise: Acquire a professional career and personal development in industries / higher studies / research assignments / entrepreneurs.

PEO2. Life-long learning: Sustain to develop their knowledge and skills throughout their career.

PEO3. Ethical Knowledge: Exhibit professionalism, ethical attitude, communication skills, teamwork and adapt to Current trends.

Programme Outcomes (Pos) – Regulations 2023

On successful completion of B.E. Electronics Engineering (VLSI Design and Technology) programme, graduating students/graduates will be able to:

1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/Development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct Investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Lifelong Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcomes (PSOs) – Regulations 2023

On successful completion of B.E. Electronics and Communication Engineering programme, graduating students/graduates will be able to:

PSO1: Technology deployment: Graduates will be capable of designing and implementing VLSI circuits utilizing appropriate design methodologies and optimization techniques

PSO2: IC design: Graduates will possess the ability to design ICs with optimal performance, power consumption, and area utilization, considering factors such as noise, timing, and signal integrity

Dr. Mahalingam College of Engineering and Technology, Pollachi
2023 Regulation - Course Code Generation Procedure for UG Courses

Regulation

Mode of Assessment	
Character Type – Number	
T	Theory
I	Theory with Practical
L	Practical
	Practical with Theory
E	Elective
O	Open Elective
P	Project
S	Skill Development Course/Internship
C	Customized

Semester Number	
Character Type – Number	
1 to 8	Semester
0	Floating

Sequence Number
Character Type – Number
01, 02, 03, . . . , 99

1	2	3	4	5	6	7	8
2	3	A	U	X	X	0	1

Board/Department/Programme/Course Type			
Character Type – Alphabet			
AD	Artificial Intelligence & Data Science	**ME**	Mechanical
AM	CSE (Artificial Intelligence & Machine Learning)	**SC**	CSE (Cyber Security)
AU	Automobile	**PH**	Physics
CE	Civil	**CH**	Chemistry
CS	Computer Science	**EN**	English
EA	Advanced Communication Technology	**MA**	Mathematics
EC	Electronics and Communication	**ES**	Employability Skills
EE	Electrical and Electronics	**VA**	Value Added Course
EV	VLSI Design & Technology	**SA**	Studio Activities
IT	Information Technology		

Dr. MAHALINGAM COLLEGE OF ENGINEERING AND TECHNOLOGY
Affiliated to Anna University, Chennai; Approved by AICTE ; Accredited by NAAC with Grade 'A++'
Accredited by NBA - Tier1 (Mech, Auto, Civil, EEE, ECE, E&I and CSE)
Udumalai Road, Pollachi - 642 003. Tel: 04259-236030/40/50 Fax: 04259-236070 www.mcet.in

Programme: B.E. Electronics Engineering (VLSI Design and Technology)

2023 Regulation

Curriculum for Semester I to VII
(2024 Batch onwards)

Course Category	Course Code	Course Title	Duration	Credits	Marks
VAC	23VAL101	Induction Program	3 Weeks	-	100

Semester I

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
AEC	23ENI101	Communication Skills I	2	0	2	3	100	All
Minor	23MAI102	Matrices and Calculus	3	0	2	4	100	AU,EA,EC, EE,EV&ME
Minor	23PHI101	Semiconductor Physics	3	0	2	4	100	-
Major	23ECT101	Electron Devices and Applications	3	0	0	3	100	-
Multi-disciplinary	23ADT001	C Programming	3	0	0	3	100	CE,EA,EC&EV
Multi-disciplinary	23ADL001	C Programming Laboratory	0	0	3	1.5	100	CE,EA,EC&EV
VAC	23VAL102	Wellness for Students	0	0	2	1	100	All
VAC	23VAT101	தமிழர்மரபு /Heritage of Tamils	1	0	0	1	100	All
AEC	23SAL101	Studio Activities	0	0	2	-	-	All
		Total	**15**	**0**	**15**	**20.5**	**800**	-

Semester II

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
AEC	23ENI201/ 23FLT201/ 23FLT202	Communication Skills II/ Foreign Language – Japanese/ Foreign Language – German	2	0	2	3	100	All
			3	0	0			
			3	0	0			
Minor	23MAI202	Complex Variables and Transforms	3	0	2	4	100	AU,EC,EE, EV&ME
Minor	23CHI202	Chemistry for Electronics Engineering	3	0	2	4	100	-
Multi-disciplinary	23ITT202	Problem Solving and Python Programming	3	0	0	3	100	EA,EC&EV
Multi-disciplinary	23MEL001	Engineering Drawing	1	0	3	2.5	100	AD,AM,AU,CS,EA,EC,EE,EV,IT,ME&SC
SEC	23ESL201	Professional Skills 1:Problem solving skills & Logical Thinking	0	0	2	1	100	All
VAC	23VAT201	தமிழரும் தொழில்நுட்பமும் / Tamils and Technology	1	0	0	1	100	All
Multi-disciplinary	23CHT202	Environmental Sciences	1	0	0	-	100	All
AEC	23SAL201	Studio Activities	0	0	2	-	-	All
		Total	**14**	**0**	**13**	**18.5**	**800**	-

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025

BoS Chairman

Semester III

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Minor	23MAT303	Numerical Techniques and Linear Algebra	3	1	2	4	100	-
Major	23EVT301	Circuit Theory and Network Analysis	3	0	0	3	100	--
Major	23EVT302	Analog Electronics	3	0	0	3	100	--
Major	23EVT303	Digital Electronics	3	0	0	3	100	--
Multi-Disciplinary	23EVI301	Data Structures and Algorithms using Python	2	0	2	3	100	-
Major	23ECL301	Analog Electronics Laboratory	0	0	3	1.5	100	--
Major	23ECL302	Digital Electronics Laboratory	0	0	3	1.5	100	--
SEC	23ESL301	Professional Skills 2: Problem solving skills & Logical Thinking 2	0	0	2	1	100	All
VAC	23VAT301	Universal Human Values 2 :Understanding Harmony	2	1	0	3	100	All
AEC	23SAL301	Studio Activities	0	0	2	-	-	All
		Total	**16**	**1**	**14**	**23**	**900**	-

Semester IV

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Minor	23MAI401	Probability Theory and Statistics	3	0	2	4	100	-
Major	23EVT401	Signals and Systems	3	1	0	4	100	-
Major	23EVT402	Linear Integrated Circuits	3	0	0	3	100	-
Major	23EVT403	Microprocessors and Microcontrollers	3	0	0	3	100	-
Major	23EVI404	Fundamentals of VLSI	3	0	2	4	100	-
Major	23EVL401	Linear Integrated Circuits Laboratory	0	0	4	2	100	-
Major	23EVL402	Microprocessors and Microcontrollers Laboratory	0	0	4	2	100	-
SEC	23ESL401	Professional Skills 3 : Professional Development and Etiquette	0	0	2	1	100	All
AEC	23SAL401	Studio Activities	0	0	2	-	-	All
		Total	**15**	**1**	**16**	**23**	**800**	-

Course Category	Course Code	Course Title	Duration	Credits	Marks
SEC	23EVSXXX	Internship – 1/Community Internship /Skill Development	2 Weeks	**1**	**100**

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025

BoS Chairman

Semester V

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVT501	Control Systems	3	1	0	4	100	-
Major	23EVT502	HDL Programming	3	0	0	3	100	-
Major	23EVT503	Analog IC Design	3	0	0	3	100	-
Major	23XXXXX	Professional Elective – I	3	0	0	3	100	-
Major	23XXXXX	Professional Elective – II	3	0	0	3	100	-
Major	23EVL501	HDL Programming Laboratory	0	0	3	1.5	100	-
Major	23EVL502	Analog IC Design Laboratory	0	0	3	1.5	100	-
SEC	23ESL501	Professional Skills 4: Communication Skills and Interview Essentials	0	0	2	1	100	All
Project	23EVP501	Reverse Engineering Project	0	0	6	3	100	All
AEC	23SAL501	Studio Activities	0	0	2	-	-	All
		Total	**15**	**1**	**16**	**23**	**900**	**-**

Semester VI

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVT601	Digital IC Design	3	0	0	3	100	--
Major	23EVT602	VLSI Digital Signal Processing	3	0	0	3	100	--
Major	23EVT603	FPGA based System Design	3	0	0	3	100	--
Major	23XXXXXX	Professional Elective – III	3	0	0	3	100	--
Major	23XXXXXX	Professional Elective – IV	3	0	0	3	100	--
Minor	23XXXXXX	Open Elective – I	3	0	0	3	100	--
Major	23EVL601	Digital IC Design Laboratory	0	0	3	1.5	100	--
Major	23EVL602	FPGA based System Design Laboratory	0	0	3	1.5	100	--
SEC	23ESL601	Professional Skills 5: Ace and Elevate : Aptitude and Soft Skills	0	0	2	1	100	All
AEC	23SAL601	Studio Activities	0	0	2	-	-	All
		Total	**18**	**0**	**9**	**22**	**900**	

Course Category	Course Code	Course Title	Duration	Credits	Marks
SEC	23EVSXXX	Internship – 2/ Research Internship/ Skill Development	2 Weeks – 4 Weeks	**1**	**100**

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025

BoS Chairman

Tentative Curriculum for Semester VII to VIII

Semester VII

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVT701	ASIC Design	3	0	0	3	100	--
Major	23EVT702	Verification and Testing	3	0	0	3	100	--
Major	23EVE005	Professional Elective - V	3	0	0	3	100	--
Major	23EVE006	Professional Elective - VI	3	0	0	3	100	--
Minor	23EVO002	Open Elective - II	3	0	0	3	100	--
Major	23EVL701	Verification and Testing Laboratory	0	0	3	1.5	100	--
Project	23EVP701	Project Phase - I	0	0	8	4	100	--
Total			15	0	11	20.5	700	

Semester VIII

Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Project	23EVP801	Project Phase – II	0	0	12	6	200	Project
Internship	23EVSXXX	Internship – 3	8 Weeks			4	100	
Total			**0**	**0**	**12**	**10**	**300**	

Total Credits: 163.5

Vertical wise Electives

Vertical I - Semiconductor Technologies and Packaging Systems								
Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVE001	Advanced MOSFET Modelling	3	0	0	3	100	-
Major	23EVE002	Compound Semiconductor Devices	3	0	0	3	100	-
Major	23EVE003	Design of Analog Filters and Signal Conditioning Circuits	3	0	0	3	100	-
Major	23EVE004	Signal Integrity for High-Speed Design	3	0	0	3	100	-
Major	23EVE005	Electronic Packaging Techniques	3	0	0	3	100	-
Major	23EVE006	Network on Chip	3	0	0	3	100	-

Vertical II- Mixed-Signal and System Level Design								
Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVE007	Art of Analog Layout	3	0	0	3	100	-
Major	23EVE008	Mixed-Signal Circuit Design	3	0	0	3	100	-
Major	23EVE009	Data Converters	3	0	0	3	100	-
Major	23EVE010	Power Management and Clock Distribution Circuits	3	0	0	3	100	-
Major	23EVE011	Radio Frequency IC Design	3	0	0	3	100	-
Major	23EVE012	PCB and System Design	3	0	0	3	100	-

Vertical III - VLSI Design Automation								
Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVE013	Scripting language for VLSI	3	0	0	3	100	-
Major	23EVE014	Algorithms for VLSI	3	0	0	3	100	-
Major	23EVE015	Physical Design and Automation	3	0	0	3	100	-
Major	23EVE016	Reconfigurable Computing System and Applications	3	0	0	3	100	-
Major	23EVE017	Machine Learning in VLSI Design	3	0	0	3	100	-
Major	23EVE018	Hardware Security and Cryptography	3	0	0	3	100	-

Vertical IV - Low Power and Quantum VLSI Systems								
Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVE019	Introduction to VLSI Life Cycle	3	0	0	3	100	-
Major	23EVE020	VLSI Technology	3	0	0	3	100	-
Major	23EVE021	Memory Devices and Circuits	3	0	0	3	100	-
Major	23EVE022	Low Power VLSI Design Techniques	3	0	0	3	100	-
Major	23EVE023	System on Chip	3	0	0	3	100	-
Major	23EVE024	Quantum Technology for Electronics Engineers	3	0	0	3	100	-

Vertical V - Embedded Intelligence and IoT Technologies								
Course Category	Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
			L	T	P			
Major	23EVE025	Embedded Systems	3	0	0	3	100	-
Major	23EVE026	IoT Processor	3	0	0	3	100	-
Major	23EVE027	Embedded System Design with FPGA	3	0	0	3	100	-
Major	23EVE028	Embedded Artificial Intelligence	3	0	0	3	100	-
Major	23EVE029	Data Analytics for IOT	3	0	0	3	100	-
Major	23EVE030	Privacy and Security in IOT	3	0	0	3	100	-

Diversified							
Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
		L	T	P			
23ECE051	Computer Architecture	3	0	0	3	100	EA,EC,EV
23EEE085	Industrial Automation	3	0	0	3	100	EA,EC,EE,EV
23EEE014	Automotive Electronics	3	0	0	3	100	EA,EC,EE,EV
23MEE008	PLM for Engineers	2	0	2	3	100	Common to all
23MEE030	Principles of Management	3	0	0	3	100	EA,EC,EV,ME
23SCE050	Cybersecurity	3	0	0	3	100	-
23AUE050	Entrepreneurship Development	3	0	0	3	100	Common to all
23AUE051	Design Thinking and Innovation	3	0	0	3	100	Common to all
23ITE047	Intellectual Property Rights	3	0	0	3	100	Common to all

Open Elective							
Course Code	Course Title	Hours/Week			Credits	Marks	Common to Programmes
		L	T	P			
23EVO001	Microelectronics	3	0	0	3	100	-
23EVO002	Nanoelectronics	3	0	0	3	100	-

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

SEMESTER I

Course Code: 23VAL101	Course Title: Induction Program (Common to all B.E/B.Tech Programmes)	
Course Category: VAC	Course Level: Introductory	
Duration: 3 Weeks	Mandatory Non- Credit Course	Max Marks: 100

Pre–requisites

- **Nil**

Course Objectives:

The course is intended to

1. Explain various sources available to meet the needs of self, such as personal items and learning resources
2. Explain various career opportunities, opportunity for growth of self and avenues available in the campus
3. Explain the opportunity available for professional development
4. Build universal human values and bonding amongst all the inmates of the campus and the society.

Module I **22 Hours**

List of Activities:

1. History of Institution and Management: Overview on NIA Educational Institutions – Growth of MCET – Examination Process –OBE Practices –Code of Conduct – Centre of Excellence.
2. Lectures, interaction sessions and Motivational Talks by Eminent people, Alumni, Employer and Industry Experts
3. Familiarisation of Department / Branch: HoD's & Senior Interaction- Department Association
4. Universal Human Value Modules : Aspirations and concerns, Self-Management, Relations Social and Natural Environment.
5. Orientation on Professional Skills Courses
6. Proficiency Modules : Mathematics, English, Physics and Chemistry
7. Introduction to various Chapters, Cells, Clubs, and its events
8. Creative Arts : Painting, Music, and Dance
9. Physical Activity :Games, Sports, and Yoga
10. Group Visits: Visit to local area and Campus Tour

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Explain various sources available to meet the needs of self, such as personal items and learning resources through visit to local areas and campus	Understand
CO 2: Explain various career opportunities and avenues available in the campus through orientation sessions	Understand
CO 3: Explain the opportunity available for professional development through professional skills, curricular, co-curricular and extracurricular activities	Understand
CO 4: Build universal human values and bonding amongst all the inmates of the campus and society for having a better life	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	-	-	-	-	-	-	2	1	2	-	-	-	-
CO2	1	-	-	-	-	-	-	2	1	2	-	-	-	-
CO3	1	-	-	-	-	-	-	2	1	2	-	-	-	-
CO4	2	-	-	-	-	-	-	2	1	2	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Reading material, Workbook prepared by PS team of the college

Reference Book(s):

R1. Sean Covey, “Seven habits of highly effective teenagers”, Simon & Schuster Uk, 2004.

R2. Vethathiri Maharishi Institute For Spiritual and Intuitional Education, aliyar, “value educat harmonious life (Manavalakalai Yoga)”, Vethathri Publications, Erode, 2010.

R3.Dr.R.Nagarathna, Dr.H.R. Nagendra, “ Integrated approach of yoga therapy for positive Swami Vivekananada Yoga Prakashana Bangalore,2008 Ed.

Web References:

1. https://youtube.com/playlist?list=PLYwzG2fd7hzc4HerTNkc3pS_IvcCfKznV
2. https://www.youtube.com/watch?v=P4vjfEVk&list=PLWDeKF97v9SO0frdgmpaghDMjkom1
3. https://fdp-si.aicte-india.org/download/AboutSIP/About%20SIP.pdf

Course Code: 23ENI101		Course Title: Communication Skills I (Common to all B.E/B.Tech Programmes)	
Course Category: AEC		Course Level: Introductory	
L:T:P(Hours/Week) 2:0:2	Credits: 3	Total Contact Hours: 60	Max Marks:100

Course Objectives:

The course is intended to impart formal and informal language effectively and accurately in various real-life contexts on par with B1 level of CEFR Scale.

Module I **20 Hours**

Grammar: Synonyms & Antonyms -Tense forms - Modals - Passives – Reported Speech – Comparatives and Descriptive adjectives.

Listening: Listening for gist and specific information - Listening to past events, experiences, and job preferences - Listening to descriptions of monuments - Listening for excuses - Listening to description: transportation systems and public places.

Speaking: Introducing oneself - Exchanging personal information – Effective Conversations: Role Play Situations (Describing personality traits - Describing landmarks, monuments, and festivals - Making polite requests and excuses - Discussing facts - Asking for and giving information – Expressing wishes - Talking about lifestyle changes - Talking about transportation and its problems - Describing positive and negative features of things and places - Making comparisons)

Reading: Skimming and Scanning - Reading Comprehension - Reading and comprehending online posts and emails – Case Studies

Writing: Letter writing (Permission letters - Online cover letter for job applications) - Instructions - Recommendations - Write a blog (General) - Report Writing (Industrial Visit Report and Event Reports) - formal and informal emails.

Module II **20 Hours**

Grammar: Sequence adverbs - Phrasal verbs - Relative clauses – Imperatives - Infinitives - Conditionals.

Listening: Listening to review of food items - Listening to results of surveys- Listening to motivational talks & podcasts

Speaking: Expressing likes and dislikes - Describing a favourite snack - Giving advices and suggestions - Speculating about past and future Events – Group Discussion

Reading: Reading different expository texts - Reading to factual texts - Print and online media Reading Comprehension

Writing: Process Descriptions – Email Writing (Requesting for information) - Reviewing Movie – Social media feeds/posts (Any social media)

List of Experiments: **20 Hours**

1. Mini Presentation and Picture Prompt Discussion
2. Debate Tournament
3. Listening, Mind Mapping & Summarization
4. Listening to Stories and Providing the Innovative Climax
5. Reading Comprehension
6. Writing - Interpretation of Visuals

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO 1: Utilize the basic English grammar and vocabulary to acquire professional communication skills.	Apply
CO 2: Develop listening and speaking skills through classroom activities based on listening comprehension, recapitulation, interpretation, and debate on the same	Apply
CO 3: Read and write social media posts and comments	Apply
CO 4: Perform as a member of a team and engage in individual presentation	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO2	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO3	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO4	-	-	-	-	-	-	-	-	2	3	-	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Jack C. Richards, Jonathan Hull, and Susan Proctor, “Interchange - Student’s book 2”, 5thEdition, Cambridge University Press, South Asia Edition, 2022.

T2. Jack C. Richards, Jonathan Hull, and Susan Proctor, “Interchange - Student’s Book 1”, 5thEdition, Cambridge University Press, South Asia Edition, 2022.

Reference Book(s):

R1. David Bohlke, Jack C. Richards, “Four Corners”, 2nd Edition, Cambridge University Press,2018.

R2. Adrian Doff, Craig Thaine, Herbert Puchta, Jeff Stranks, Peter Lewis-Jones, Graham Burton, Empower B1 – Student’s Book, Cambridge University Press, 2020.

R3. Raymond Murphy, “Intermediate English Grammar” 30th Edition, Cambridge University Press,2022.

Web References:

1. https://speakandimprove.com/
2. https://writeandimprove.com/
3. https://www.cambridgeenglish.org/exams-and-tests/linguaskill/

Course Code: 23PHI101		Course Title: Semiconductor Physics	
Course Category: Minor		Course Level: Introductory	
L: T:P (Hours/Week) 3:0:2	Credits: 4	Total Contact Hours: 75	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on the fundamentals of semiconductor physics and discuss the working and applications of few basic devices.

Module I **22 Hours**

Semiconductors: Energy Band and Charge Carriers: Energy bands in semiconductors, Types of semiconductors, Charge carriers, Intrinsic and extrinsic materials. Carrier concentration: Fermi Level, Electron and hole concentration equilibrium, Temperature dependence of carrier concentration, Compensation, and charge neutrality. Conductivity and mobility, Effect of temperature, Doping and high electric field.

Optical Excitation in Semiconductor: Optical absorption, carrier generation, Carrier life time, diffusion length and photo conductivity, Direct and indirect recombination and trapping, Photoconductive devices. Diffusion of carriers, Einstein relation, Continuity equation, Carrier injection, Diffusion length. Haynes-Shockley experiment.

Module II **23 Hours**

Junctions: p-n junction and contact potential, Fermi levels, Space charge, Reverse and Forward bias, Zener, and Avalanche breakdown. Capacitance of p-n junction, Schottky barriers; Schottky barrier height, C-V characteristics, current flow across Schottky barrier: thermionic emission, Rectifying contact, and Ohmic contact.

Photonics: LED: Radiative transition, Emission spectra, Luminous efficiency and LED materials, Solar cell, and photodetectors: Ideal conversion efficiency, Fill factor, Equivalent circuit, V_{oc}, I_{sc} and Load resistance, Spectral response. Reverse saturation current in photodetector**.**

List of Experiments: **30 Hours**

1. Determination of band gap of semiconductor
2. Determination of resistance illumination characteristics of LDR
3. V-I Characteristics of PN Junction diode
4. V-I Characteristics of Zener diode
5. V-I Characteristics of LED
6. V-I Characteristics of Solar cell
7. V-I Characteristics of Photodiode

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Interpret the basic properties of semiconductors including the band gap, charge carrier concentration, doping and charge carrier injection/excitation.	Apply
CO 2: Adapt the fundamentals of semiconductors in explaining the design consideration and working of p-n junctions.	Apply
CO 3: Utilize the concept of p-n junction in the design considerations and working of the various photonic devices like LEDs, solar-cells, and photodetectors.	Apply
CO 4: Conduct, analyze and interpret the data and results from the various physics laboratory experiments.	Evaluate

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	3	-	-	-	-	-	-	-	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. B. G. Streetman and S. K. Banerjee, “Solid State Electronics”, Pearson, 7th Edition, 2016.

T2. S.M. Sze and Kwok K. Ng, “Physics of Semiconductor Devices”, John Wiley, 3rd Edition, 2015.

Reference Book(s):

R1. M.S. Tyagi, “Introduction to semiconductor materials and devices”, John Wiley, 2008.

R2. Umesh K. Mishra, and Jaspreet Singh, “Semiconductor Device Physics and Design,” Springer, 2007.

R3. R. F. Pierret, “Semiconductor Device Fundamentals”, Pearson Education Inc., 2006.

Web References:

1. https://archive.nptel.ac.in/courses/108/108/108108122/
2. https://www.udemy.com/course/semiconductors-vlsi/?couponCode=IND21PM
3. https://vlab.amrita.edu/?sub=3&brch=269&sim=1371&cnt=1

Course Code: 23EVI101		Course Title: Electron Devices and Applications	
Course Category: Major		Course Level: Introductory	
L: T:P (Hours/Week) 3:0:2	Credits: 4	Total Contact Hours: 75	Max Marks:100

Course Objectives:

The course is intended to impart knowledge of basic electronic devices such as diodes, Bipolar junction Transistors and Field Effect Transistors with its applications.

Module I **23 Hours**

Semiconductor Diode: PN junction - forward and reverse bias conditions, V-I Characteristics, and its Temperature dependence – Diode specifications - Diode Resistance – Diode junction Capacitance – Transition and Diffusion capacitances - Rectifiers - Clipper - Clamper

Special Diodes: Zener diode - Characteristics of Zener diode - Avalanche and Zener breakdown - Application of Zener diode :Voltage regulator - Varactor diode, Tunnel diode, Light emitting diodes – Photo diodes

Bipolar Junction Transistors: Bipolar Junction Transistor and its types: NPN and PNP Transistor - Transistor operation - Configurations of BJT : Input and output characteristics of CE,CB and CC configurations - Transistor as a Switch and Amplifier.

Module II **22 Hours**

Field Effect Transistors: JFET and its types, construction, and operation of n-channel and p- channel JFETs – characteristics curves – FET applications – Comparison of BJT and JFET.

MOSFETS : MOSFETs: Depletion MOSFETs and Enhancement MOSFETs – construction and operation - Drain and Transfer characteristics - Differences between JFETs and MOSFETs – Precaution in handling MOSFETs - MOSFET as a switch.

List of Experiments: **30 Hours**

1. Half wave and Full wave Rectifier circuits
2. Regulator using Zener diode
3. Wave shaping circuits: Clippers and clampers
4. 4.Characteristics of Common Emitter configuration
5. Characteristics of Common Base configuration
6. FET characteristics and its application as a switch.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Utilize the characteristics of PN diode to extract its resistance and various capacitances.	Apply
CO 2: Use PN junction and special diodes to design wave shaping circuits and voltage regulators.	Apply
CO 3: Utilize the characteristics of BJT and MOSFETs to design switches and amplifiers.	Apply
CO 4: Design rectifiers, voltage regulators and wave shaping circuits using PN and special diodes (for laboratory components only).	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	2	-	-	-	3	-	1	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Millman J. , Halkias C. C. "Electronic Devices and Circuits ",4th edition Tata McGraw Hill, New Delhi, 2011.

Reference Book(s):

R1. Salivahanan.S, Suresh kumar.N and Vallavaraj.A, “Electronic Devices and Circuits”, 2nd edition, TMH, New Delhi, 2008.

R2. Robert Boylestad and Louis Nashelsky, “Electron Devices and Circuit Theory”, Pearson Prentice Hall, 10th edition, 2008.

R3. Streetman Ben G. and Banerjee Sanjay, “Solid State Electronic devices”, PHI, 6th dition, 2006

R4. David A. Bell, “Electronic Devices and Circuits”, Oxford University Press, 5th edition, 2008

Web References:

1. http://nptel.ac.in/video.php?subjectId=117103063
2. http://nptel.ac.in/video.php?subjectId=117106091
3. www.youtube.com/watch?v=Wf19II0ts84

Course Code: 23ADT001		Course Title: C Programming (Common to CE, EA, EC&EV)	
Course Category: Multi-disciplinary		Course Level: Introductory	
L:T:P(Hours/Week) 3: 0:0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course helps to understand the structured and procedural programming skills. The major objective is to provide students with understanding of code organization and functional hierarchical decomposition using complex data types.

Module I **22 Hours**

Basics Of Computer Organization: Generation and Classification of Computers – Basic Organization of a Computer – Software development life cycle – Problem Solving Techniques, Algorithm, Pseudo code and Flow Chart.

Introduction To C Programming: Introduction – Structure of a C program – Keywords – Identifiers – Constants – Variables – Data Types – Operators and Expressions – Formatted & Unformatted I/O functions – Decision statements – Loop control statements.

Arrays: Characteristics – Declaration- One-dimensional array, Two-dimensional arrays

Module II **23 Hours**

Functions: Declaration & Definition of function – Built in function – User defined function -Types of functions – Call by value & reference.

Strings and Pointers: Formatting strings – String handling functions. Pointers: Features and Types of pointers – Arithmetic operations with pointers–Pointers and Arrays- Array of Pointers- Pointers and Strings

Structures and Union: Structures: Features – Operations on Structures – Array of structures – Pointers to Structures -Unions-Union of Structures.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Correlate the fundamental concepts of computer organization such as architectures of the processors and project management for real time application	Apply
CO 2: Infer the fundamental concepts of programming, such as variables, data types and control structures for real time problems	Analyze
CO 3: Apply programs solving skills and knowledge of C programming constructs to solve the given one dimensional and two dimensional datasets	Apply
CO 4: Build a module to solve the given application using functions	Apply
CO 5: Develop a program by accessing the address of the variable using pointers and manipulation of characters using string handling functions	Apply
CO 6: Test the performance of the students by group assignments and projects on real time problems	Evaluate

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-	2	-	-	-	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	2	-	1	-	-	-	-	-	-	-	-	-	-	-
CO5	3	-	-	1	-	-	-	-	-	-	-	-	-	-
CO6	-	1	-	3	2	-	-	-	2	-	-	2	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Ashok N. Kamthane, Amit.N. Kamthane, “Programming in C,” 3rd Edition, Pearson Education, 2015.

T2. Deitel H M and Deitel P J, “C How to Program”, Prentice Hall, 2013.

Reference Book(s):

R1. Ajay Mittal, “Programming in C-A Practical Approach”, 3rd Edition, Pearson Education, 2010.

R2. Yashavant P.Kanetkar,” Let Us C” , 16th Edition, BPB Publications, 2018. R3. Herbert Schildt, “C The Complete Reference", Tata McGraw Hill, 2010.

R3. S Gottfried Byron, “Programming With C”, Tata McGraw Hill, 2011.

Web References:

1. NPTEL course content on Introduction to Programming In https://onlinecourses.nptel.ac.in/noc22_cs40
2. Complete guide on Learn C programming: http://www.cprogramming.com/
3. Complete reference manual on C programming: http://www.c4learn.com/

Course Code: 23ADL001		Course Title: C Programming Laboratory (Common to CE, EA, EC&EV)	
Course Category: Multi-disciplinary		Course Level: Introductory	
L: T:P (Hours/Week) 0:0:3	Credits: 1.5	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course introduces students to the practical knowledge of programming using C programming language as an implementation tool. It aims at providing students with understanding of programming essentials used within the framework of imperative and structural programming paradigms.

List of Experiments: **45 Hours**

1. Implement basic C programs using data types
2. Implement programs using Operators and Expressions
3. Develop Programs using Branching statements
4. Implement Programs using Control Structures
5. Develop programs using Arrays
6. Implement programs using Functions
7. Implement programs using String Operations
8. Develop programs using Pointers
9. Implement programs using Structures
10. Develop programs using Union

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Write programs using appropriate programming constructs	Apply
CO 2: Apply programs solving skills and knowledge of C programming constructs to solve the given one dimensional and two dimensional datasets	Analyze
CO 3: Develop a program by accessing the address of the variable using pointers and manipulation of characters using string handling functions	Apply
CO 4: Evaluate modular programming techniques to break down complex programs into smaller and manageable modules	Evaluate

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	3	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	3	-	-	-	-	-	-	-	-	-
CO3	-	2	-	-	3	-	-	-	-	-	-	-	-	-
CO4	-	-	-	3	3	-	-	-	-	-	-	1	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Ashok N. Kamthane, Amit.N. Kamthane, “Programming in C,” 3rd Edition, Pearson Education, 2015.

T2. Deitel H M and Deitel P J, “C How to Program”, Prentice Hall, 2013.

Reference Book(s):

R1. Ajay Mittal, “Programming in C-A Practical Approach”, 3rd Edition, Pearson Education, 2010.

R2. Yashavant P.Kanetkar,” Let Us C” , 16th Edition, BPB Publications, 2018. R3. Herbert Schildt, “C The Complete Reference", Tata McGraw Hill, 2010.

Web References:

1. C programming resources: https://electronicsforu.com/resources/15-free-c-programming-ebooks
2. C programming tutorials: https://www.fromdev.com/2013/10/c-programming-tutorials.html
3. C Manual: https://books.goalkicker.com/CBook

Course Code: 23VAL102		Course Title: Wellness for Students (Common to all B.E/B.Tech Programmes)	
Course Category: VAC		Course Level: Introductory	
L:T:P(Hours/Week) 0:0:2	Credits: 1	Total Contact Hours: 30	Max Marks: 100

Course Objectives:

The course is intended to impart knowledge on setting SMART goals for academic, career and life, applying time management techniques, articulating the importance of wellness for success in life and understanding the dimensions of wellbeing and relevant practices.

Module I **15 Hours**

GOAL SETTING Understanding Vision and mission statements - Writing personal mission statements – 'Focus' as a way of life of most successful people. Clarifying personal values, interests, and orientations – Awareness of opportunities ahead – Personal SWOT analysis - Principles driving goal setting: Principle of response and stimuli, Circle of influence and circle of concern, what you see depends on the role you assume. Potential obstacles to setting and reaching your goals - Five steps to goals setting: SMART goals, Inclusive goals, Positive stretch, Pain vs gain, Gun-point commitment.

TIME MANAGEMENT - TOOLS AND TECHNIQUES Importance of planning and working to time. Pareto 80-20 principle of prioritization – Time quadrants as a way to prioritize weekly tasks – The glass jar principle - Handling time wasters – Assertiveness, the art of saying 'NO' – Managing procrastination.

Module II **15 Hours**

Simplified Physical Exercises. Fitness as a subset of Wellness – health related physical fitness - skill related physical fitness. Joint movements, Warm up exercises, simple asanas, WCSC simplified exercises.

PRACTICES FOR MENTAL WELLNESS

Meditation: Mind and its functions - mind wave frequency – Simple basic meditation – WCSC meditation and introspection tables. Greatness of friendship and social welfare – individual, family and world peace – blessings and benefits.

Food & sleep for wellness: balanced diet - good food habits for better health (anatomic therapy) – hazards of junk food - food and the gunas.

PUTTING INTO PRACTICE

Practical's: Using the weekly journal – Executing and achieving short term goals – Periodic reviews.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Set well-articulated goals for academics, career, and personal aspirations	Apply
CO 2: Apply time management techniques to complete planned tasks on time	Apply
CO 3: Explain the concept of wellness and its importance to be successful in career and life	Apply
CO 4: Explain the dimensions of wellness and practices that can promote wellness	Apply
CO 5: Demonstrate the practices that can promote wellness	Valuing

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	1	1	-	1	-	-
CO2	-	-	-	-	-	-	-	-	1	-	1	1	-	-
CO3	-	-	-	-	-	-	-	-	1	-	-	1	-	-
CO4	-	-	-	-	-	-	-	-	1	-	-	1	-	-
CO5	-	-	-	-	-	1	1	-	1	-	-	1	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Reading material, workbook and journal prepared by PS team of the college

Reference Book(s):

R1. Stephen R Covey, “First things first”, Simon & Schuster UK, Aug 1997

R2. Sean Covey, “Seven habits of highly effective teenagers”, Simon & Schuster UK, 2004.

R3. Vethathiri Maharishi Institute for Spiritual and Intuitional Education, Aliyar, “Value education for harmonious life (Manavalakalai Yoga)”, Vethathiri Publications, Erode, I Ed. (2010).

R4. Dr. R. Nagarathna, Dr. H.R. Nagendra, “Integrated approach of yoga therapy for positive health”, Swami Vivekananda Yoga Prakashana, Bangalore, 2008 Ed.

R5. Tony Buzan, Harper Collins, “The Power of Physical Intelligence English”

Course Code: 23VAT101		Course Title: HERITAGE OF TAMILS (Common to all B.E/B.Tech Programmes)	
Course Category: VAC		Course Level: Introductory	
L:T:P(Hours/Week) 1:0:0	Credits: 3	Total Contact Hours: 15	Max Marks: 100

Pre-requisites: NIL

Course Objectives:

மாணவர்கள் இப்பாடத்தை கற்றலின் மூலம்

CO.1 மொழி மற்றும் இலக்கியம், பாறை ஓவியங்கள் முதல் நவீன ஓவியங்கள் வரை - சிற்பக் கலை, நாட்டுப்புறக் கலைகள் மற்றும் வீர விளையாட்டுகள், திணைக் கோட்பாடுகள் மூலம் தமிழர் மரபை அறிந்து கொள்ள இயலும்.

CO.2 இந்திய தேசிய இயக்கம் மற்றும் இந்திய பண்பாட்டிற்குத் தமிழர்களின் பங்களிப்பை அறிந்து கொள்ள இயலும்.

தமிழர் மரபு

அலகு 1- மொழி மற்றும் இலக்கியம் **3 Hours**

இந்திய மொழிக் குடும்பங்கள் - திராவிட மொழிகள் - தமிழ் ஒரு செம்மொழி - தமிழ் செவ்விலக்கியங்கள் - சங்க இலக்கியத்தின் சமயச் சார்பற்ற தன்மை - சங்க இலக்கியத்தில் பகிர்தல் அறம் - திருக்குறளில் மேலாண்மைக் கருத்துக்கள் - தமிழ்க் காப்பியங்கள், தமிழகத்தில் சமண பௌத்த சமயங்களின் தாக்கம் - பக்தி இலக்கியம், ஆழ்வார்கள் மற்றும் நாயன்மார்கள் சிற்றிலக்கியங்கள் - தமிழில் நவீன இலக்கியத்தின் வளர்ச்சி - தமிழ் இலக்கிய வளர்ச்சியில் பாரதியார் மற்றும் பாரதிதாசன் ஆகியோரின் பங்களிப்பு.

அலகு 2 - மரபு - பாறை ஓவியங்கள் முதல் நவீன ஓவியங்கள் வரை - சிற்பக் கலை **3 Hours**

நடுகல் முதல் நவீன சிற்பங்கள் வரை - ஐம்பொன் சிலைகள் - பழங்குடியினர் மற்றும் அவர்கள் தயாரிக்கும் கைவினைப் பொருட்கள், பொம்மைகள் - தேர் செய்யும் கலை - சுடுமண் சிற்பங்கள் - நாட்டுப்புறத் தெய்வங்கள் - குமரிமுனையில் திருவள்ளுவர் சிலை - இசைக் கருவிகள் - மிருதங்கம், பறை, வீணை, யாழ், நாதஸ்வரம் - தமிழர்களின் சமூக பொருளாதார வாழ்வில் கோவில்களின் பங்கு.

அலகு 3 - நாட்டுப்புறக் கலைகள் மற்றும் வீர விளையாட்டுகள் **3 Hours**

தெருக்கூத்து, கரகாட்டம், வில்லுப்பாட்டு, கணியான் கூத்து, ஒயிலாட்டம், தோல்பாவைக் கூத்து, சிலம்பாட்டம், வளரி, புலியாட்டம், தமிழர்களின் விளையாட்டுகள்.

அலகு 4 - தமிழர்களின் திணைக் கோட்பாடுகள் **3 Hours**

தமிழகத்தின் தாவரங்களும், விலங்குகளும் - தொல்காப்பியம் மற்றும் சங்க இலக்கியத்தில் அகம் மற்றும் புறக் கோட்பாடுகள் - தமிழர்கள் போற்றிய அறக் கோட்பாடு சங்க காலத்தில் தமிழகத்தில் எழுத்தறிவும், கல்வியும் - சங்ககால நகரங்களும் துறைமுகங்களும் - சங்க காலத்தில் ஏற்றுமதி மற்றும் இறக்குமதி - கடல் கடந்த நாடுகளில் சோழர்களின் வெற்றி.

அலகு 5 - இந்திய தேசிய இயக்கம் மற்றும் இந்திய பண்பாட்டிற்குத் தமிழர்களின் பங்களிப்பு **3 Hours**

இந்திய விடுதலைப் போரில் தமிழர்களின் பங்கு இந்தியாவின் பிறபகுதிகளில் தமிழ்ப் பண்பாட்டின் தாக்கம் - சுய மரியாதை இயக்கம் - இந்திய மருத்துவத்தில் சித்த மருத்துவத்தின் பங்கு - கல்வெட்டுகள், கையெழுத்துப் படிகள்- தமிழ்ப் புத்தகங்களின் அச்சு வரலாறு.

Course Outcomes	**Cognitive Level**
மாணவர்கள் இப்பாடத்தை கற்றபின்	
CO1: மொழி மற்றும் இலக்கியம், பாறை ஓவியங்கள் முதல் நவீன ஓவியங்கள் வரை - சிற்பக் கலை, நாட்டுப்புறக் கலைகள் மற்றும் வீர விளையாட்டுகள், திணைக் கோட்பாடுகள் மூலம் தமிழர் மரபை அறிந்து கொள்வார்கள்.	அறிதல் (Understand)
CO2: இந்திய தேசிய இயக்கம் மற்றும் இந்திய பண்பாட்டிற்குத் தமிழர்களின் பங்களிப்பை அறிந்து கொள்வார்கள்	அறிதல் (Understand)

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	1	-	-
CO2	-	-	-	-	-	-	-	-	-	-	-	1	-	-

High-3; Medium-2; Low-1

Text Cum Reference Book(s):

1. தமிழக வரலாறு - மக்களும் பண்பாடும் -கே.கே.பிள்ளை (வெளியீடு. தமிழ்நாடு பாடநூல் மற்றும் கல்வியியல் பணிகள் கழகம்)
2. கணினித் தமிழ் - முனைவர் இல. சுந்தரம் (விகடன் பிரசுரம்)
3. கீழடி - வைகை நதிக்கரையில் சங்க கால நகர நாகரிகம் (தொல்லியல் துறை வெளியீடு
4. பொருநை - ஆற்றங்கரை நாகரிகம் (தொல்லியல் துறை வெளியீடு
5. Social Life of Tamils (Dr.K.K.Pillay) A joint publication of TNTB & ESC and RMRL (in print)
6. Social Life of the Tamils - The Classical Period (Dr.S.Singaravelu) (Published by: International Institute of Tamil Studies.
7. Historical Heritage of the Tamils (Dr.S.V.Subatamanian, Dr.K.D. Thirunavukkarasu) (Published by: International Institute of Tamil Studies).
8. The Contributions of the Tamils to Indian Culture (Dr.M.Valarmathi) (Published by: International Institute of Tamil Studies.)
9. Keeladi - 'Sangam City Civilization on the banks of river Vaigai' (Jointly Published by: Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation, Tamil Nadu)
10. Studies in the History of India with Special Reference to Tamil Nadu (Dr.K.K.Pillay) (Published by: The Author)
11. Porunai Civilization (Jointly Published by: Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation, Tamil Nadu)
12. Journey of Civilization Indus to Vaigai (R.Balakrishnan) (Published by: RMRL) - Reference Book.

SEMESTER II

Course Code: 23ENI201		Course Title: Communication Skills II (Common to all B.E/B.Tech Programmes)	
Course Category: AEC		Course Level: Introductory	
L:T:P(Hours/Week) 2:0:2	Credits: 3	Total ContactHours:60	Max Marks:100

Course Objectives:

The course is intended to impart effective and accurate language in business correspondence on par with B2 level of CEFR Scale.

Module I **20 Hours**

Grammar: Linking Words - Collocations –Sentence Completion - Articles –Adverbs– Indefinite Pronoun

Listening: Listening to short conversations - Listening for gist and summarizing - Listening for detail - Responding to straightforward questions.

Speaking: Making statements of facts - Agreeing and disagreeing to opinions - Respond to queries - Group Discussion.

Reading: Read and select (phrasal verbs & relative clause)- Cloze Test - Gapped sentences - Multiple- choice gap-fill

Writing: Paragraph Writing: Descriptive, narrative, persuasive and argumentative - Emails: Giving information - Making enquiries - Responding to enquiries - Power Point Presentation

Module II **20 Hours**

Grammar: Expressions of cause and result – Concord - Error Spotting (Parts of Speech & Indian English) - Prepositions

Listening: Listening for identifying main points - Responding to a range of questions about different topics - Listening to identify relevant information

Speaking: Empathetic Enunciation – Situation handling – Visual Interpretation - - Short presentations

Reading: Intensive Reading: Comprehending business articles, reports and proposals and company websites-- Open gap-fill - Extended reading

Writing: – Report Writing - Memo – Complaint letter - Business Letters (Seeking permission & Providing Information)

List of Experiments: **20 Hours**

1. Listening to Monologue and Extended Listening Activity I
2. Listening to Monologue and Extended Listening Activity II
3. Expressing Opinions and Situational based speaking
4. Mini Presentation and Visual Interpretation
5. Reading Comprehension
6. Writing letter, email, and report

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Identify the common errors in written and spoken correspondence.	Apply
CO2: Develop listening, reading, and speaking skills through task based activities in listening, reading comprehension, recapitulation, interpretation, and discussion.	Apply
CO3: Read business correspondences like memo, Email, letter, proposals and write reports and website entries and product launches.	Apply
CO4: Perform as an individual and member of a team and engage effectively in group discussion and individual presentation.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO2	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO3	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO4	-	-	-	-	-	-	-	-	2	3	-	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Guy Brook- Hart, “Business Benchmark Upper Intermediate”, 2nd Edition, South Asian, Cambridge University Press, 2020.

T2. Norman Whitby, “Business Benchmark pre-intermediate to Intermediate”, 2nd Edition, South Asian, Cambridge University Press, 2014.

Reference Book(s):

R1. Hewings Martin - Advanced Grammar in use Upper-intermediate Proficiency, CUP,3rd Edition,2013.

R2. Clark David – Essential BULATS (Business Language Testing Service), CUP, 2006.

R3. Adrian Doff, Craig Thaine, Herbert Puchta, Jeff Stranks, Peter Lewis-Jones, Rachel Godfrey, Gareth Davies, Empower B1+ – Student’s Book, Cambridge University Press,2015.

Web References:

1. https://speakandimprove.com/
2. https://writeandimprove.com/
3. https://www.cambridgeenglish.org/exams-and-tests/linguaskill/

Course Code:23FLT201		Course Title: FOREIGN LANGUAGE -JAPANESE (Common to all B.E/B.Tech Programmes)	
Course Category: AEC		Course Level: Introductory	
L:T:P (Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max. Marks:100

Course Objectives:

The course objectives intended to:

1. Express a basic exposure on Japanese language and culture
2. Express thoughts and communicate in the beginner level of Japanese with native Japanese speaker
3. Identify the kanji etymology as well as use it in basic vocabulary required for the JLPT/NAT 5 examination level
4. Read and write 100 kanji of the official JLPT N5
5. Choose the appropriate verb forms for learning and practicing the Japanese language

Unit I Introduction to Japan and greetings 9 Hours

Japan : Land and culture - Introduction to Japanese language – Greetings – Seasons - Days of the week - Months of the year – Dates of the month - Self introduction – Numbers (Upto 99,999) – Expressing time – Conversation audio and video.

Listening: Listening to Greetings - Listening for Specific Information: Numbers, Time.

Speaking: Self-Introduction

Unit II Building vocabulary 9 Hours

Family relationships - Colours - Parts of body - Profession - Directions - Time expressions (today, tomorrow, yesterday, day before, day after) - Japanese housing and living style - Food and transport (vocabulary) - Stationery, fruits, and vegetables

Listening: Listening for Specific Information: Directions, Family Members, Parts of body Speaking: Introducing one's family.

Unit III Writing systems 9 Hours

Hiragana Chart 1 - vowels and consonants and related vocabulary – Hiragana Charts 2&3, double consonants, vowel elongation and related vocabulary – Introduction to Kanji – Basic Vocabulary – Basic Conversational Phrases.

Listening: Listening to Japanese Alphabet Pronunciation, Simple Conversation.

Speaking: Pair Activity (Day to day situational conversation)

Unit IV Kanji and preposition **9 Hours**

Katakana script and related vocabulary – Basic kanjis: naka, ue, shita, kawa , yama , numbers (1- 10, 100, 1000, 10,000 and yen) , person, man, woman, child, tree , book , hidari, migi, kuchi , 4 directions - Usage of particles wa, no, mo and ka and exercises - Usage of kore, sore, are, kono, sono, ano, arimasu and imasu - Particles – ni (location) and ga , donata and dare - Particles ni (time), kara, made , ne , koko, soko, asoko and doko - Directions : kochira, sochira, achira and dochira , associated vocabulary (mae, ushiro, ue, shita, tonari, soba, etc.)

Listening: Listening to conversation with related particles

Unit V Verb forms **9 Hours**

Introduction to Verbs - Verbs –Past tense, negative - i-ending and na-ending adjectives introduction - ~masen ka, mashou - Usage of particles de, e , o, to, ga(but) and exercises - Adjectives (present/past – affirmative and negative) – Counters - ~te form

Listening: Listening to different counters, simple conversations with verbs and adjectives.

Speaking: Pair Activity (Explaining one's daily routine by using appropriate particles and verbs)

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO 1: Recognize and write Japanese alphabet	Understand
CO 2: Comprehend the conversation and give correct meaning	Understand
CO 3: Apply appropriate vocabulary needed for simple conversation in Japanese language	Apply
CO 4: Apply appropriate grammar to write and speak in Japanese language	Apply
CO 5: Speak using words of the Japanese language	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	-	3	-	1	-	-
CO4	-	-	-	-	-	-	-	-	-	3	-	1	-	-
CO5	-	-	-	-	-	-	-	-	2	3	-	1	--	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Genki 1 Textbook: An Integrated Course in Elementary Japanese by Eri Banno, Yoko Ikeda, Yutaka Ohno, Yoko Sakane, Chikako Shinagawa, Kyoko Tokashiki published by The Japan Times

T2. Genki 1 Workbook: An Integrated Course in Elementary Japanese by Eri Banno published by The Japan Times

Reference Book(s):

R1. Japanese for Everyone: Elementary Main Textbook1-1, Goyal Publishers and Distributors Pvt. Ltd., Delhi, 2007

R2. Japanese for Everyone: Elementary Main Textbook1-2, Goyal Publishers and Distributors Pvt. Ltd., Delhi, 2007

Web References:

1. www.japaneselifestyle.com
2. www.learn-japanese.info/
3. www.learn.hiragana-katakana.com/typing-hiragana-characters/
4. www.kanjisite.com/

Course Code:23FLT202		Course Title: FOREIGN LANGUAGE -GERMAN (Common to all B.E/B.Tech Programmes)	
Course Category: AEC		Course Level: Introductory	
L:T:P (Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max. Marks:100

Course Objectives:

The course is intended to:

1. Listen and understand numbers, names and dialogues of a native speaker on par with A1 level.
2. Speak and introduce self in simple sentences to convey their opinion and ideas on par with A1 level.
3. Read simple passages and given text on par with A1 level.
4. Write letter and simple sentences on par with A1 level.

UNIT I BASIC INTRODUCTION TO GERMAN SCRIPTS 9 Hours

Theme and Text (Introduction to German - German script, Deutsche Namen, Daily Greetings and Expressions) – Grammar ('wh' questions, das Alphabet)– Speak Action (Buchstabieren, sich und andere vorstellen nach Namen und Herkunft fragen, internationale Wörter auf Deutsch verstehen, jemanden begrüßen)– pronunciation (Buchstabieren J,V,W,Y, - Long vowels A,E,I,O,U - Pronunciation of Ä,Ü,Ö) – To learn (internationale Wörter in Texten finden, Wörter sortieren) Theme and Text (Gespräche im caf'e, Getränkekarte, Telefon-buch, Namen, Rechnungen)– Grammar (Frägesatze mit wie, woher, wo, was Verben in präsens Singular und Plural, das Verb Sein, Personalpronomen und Verben)– Speak Action (eine Gespräch beginnen sich und andere vorstellen zählen, etwas bestellen und bezhalen Telefonnummern und verstehen)– pronunciation (Wortakzent in Verben und in Zahlen) – To learn (Grammatiktabelle ergänzen, mit einem Redemittelkasten arbeiten)

Unit II NUMBERS AND NOMINATIVE CASE 9 Hours

Theme and Text (Numbers – 1 to 12 (Eins bis Zwolf) – 20, 30, 40, 90 (zwanzig-Neunzig) – All Numbers (1-10000) – German Currency (Euro) – Basic Mathematics (plus, Minus, Malen, Geteilt durch)) – Grammar (Introduction of verbs –Have Verb – To Come, To Speak, To Read, To Drive, To Fly, To write, To Eat, To sleep, To take etc.,)

Theme and Text (in super market,purchase, House Maintainence, Emotion, Sports, Body parts)– Grammar (Modal Verb) – Speak Action (Body parts) – To learn (Rollenkarten arbeiten)

Marking, Umlaute ö ä ü hören und sprechen) – To learn (Lernkarten schreiben, Memotipps, eine Regel selbst finden) Theme and Text (City, Town, Language: Nachbar, Sprachen, Sehenswürdigkeiten in Europa) – Grammar (Past tense for Sein, W-Frage, Aussagesatz und Satzfrage) – Speak Action (about city and siteseeing) – pronunciation (Satzakzent in Frage- und Aussagesätzen) – To learn (eine Regel ergänzen, eine Grammatiktabelle erarbeiten, Notizen machen)

Unit III AKKUSATIVE CASE AND PREPOSITIONS 9 Hours

Theme and Text (Menschen und Hauser, Furniture catalogue, E-Mail, House information) – Grammar (possesivartikel im Nominativ, Artikel im Akkusativ, Adjektive im satz, Graduierung mit zu)– Speak Action (Whonung bescreiben about perons and things)– pronunciation (consonant - ch) – To learn (wortschatz systematisch)

Theme and Text (Termine - Appointment and punctuality in Germany) – Grammar (questions with wann?, Preposition (am, um, von. bis), verneinung mit nicht, trennbare verben, präteritum von haben) – Speak Action (Daily plan making, time commitment, excuse for late coming) – pronunciation (consonants- p,b,t,d / k,g) – To learn (Rollenkarten arbeiten)

Theme and Text (orientation in working area, go for work, floor plan city plan, office and computer) – Grammar (preposition: in,neben, unter, auf, vor, hinter, an, zwischen, bei und mit + Datic)– Speak Action (work place, work, giving appointments)– pronunciation (consonants: f,w und v) – To learn (Making notice in calender)

Unit IV DATIV CASE AND PREPOSITIONS 9 Hours

Theme and Text (Holiday and Party, holiday plan, party plan in Germany) – Grammar (regular and iregular verbs) – Speak Action (holiday speak, accident, Ich-Text schreiben) – pronunciation (lange und kurze vokale markieren) – To learn (Text Order)

Theme and Text (organising an Excursion to Berlin through city orientation, Bus plan, City plan, post card, Excursion programme) – Grammar (preposition: in, durch, über + Akkusativ: zu, an... vorbei + Dativ, Modalverb wollen) – Speak Action (Tourism, culture, postcard preparation, travel description) – pronunciation (r and l)– To learn (plaket making)Theme and Text (Beruf und all Tag, Visiten karten, wörterbuch) – Grammar – Speak Action (profession, statistic speaking) – pronunciation (n,ng and nk)– To learn (wörterbuch , text information in tabel)

Unit V ADJECTIVES AND PRONUNCIATION 9 Hours

Theme and Text (Haushaltstipp, kochrezept, maße und gewichte, Mahlzeiten und Gerichte) – Grammar (jeden Tag, manchmal, nie, Question - welche, Comparison – viel, gut, gern) – Speak Action (about eat, drink question and answers) – pronunciation (e,en,el,er) – To learn (Text auswerten und zusammenfassen)

Theme and Text (Clothing , colour, weather) – Grammar (Adjecktive im Akkusativ, unbestimmer Artikel) – Speak Action (weather, dress and colour understanding) – pronunciation (e-o- ö and ie- u- ü) – To learn (wetter and Farben interkulturelle)

Theme and Text (in super market,purchase, House Maintainence, Emotion, Sports, Body parts)– Grammar (Modal Verb) – Speak Action (Body parts) – To learn (Rollenkarten arbeiten)

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO 1: Recognize and write German alphabet, numbers.	Understand
CO 2: Comprehend the conversation and give correct meaning	Understand
CO 3: Apply appropriate grammar and vocabulary to write and speak.	Apply
CO 4: Apply appropriate cases and texts to listen, write, and speak.	Apply
CO 5: Speak and read using words of the German language	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	-	3	-	1	-	-
CO4	-	-	-	-	-	-	-	-	-	3	-	1	-	-
CO5	-	-	-	-	-	-	-	-	2	3	-	1	--	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Netzwerk, “Deutsch als Fremdsprache” by Stefanie Dengler, Paul Rusch, Helen Schmitz published

T2. Funk, Kuhn, Demme, “Studio D A1 Deutsch als Fremdsprache” published by Goyal Publishers & Distributors Pvt Ltd;

Reference Book(s):

R1. Hueber, “Fit for Goethe- Zertifikat A1 (Start Deutsch 1)” by GOYAL PUBLISHERS AND DISTRIBUTORS; 2016

Course Code: 23MAI202		Course Title: Complex Variables and Transforms	
Course Category: Minor		Course Level: Introductory	
L: T:P (Hours/Week) 3:0:2	Credits: 4	Total Contact Hours: 75	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on the fundamentals of semiconductor physics and discuss the working and applications of few basic devices.

Module I **23 Hours**

Vector Calculus

Gradient – Divergence – Curl – Line integrals – Surface integrals – Volume integrals – Theorems of Green, Gauss and Stokes (without proof) and their applications.

Complex Variables (Differentiation)

Cauchy-Riemann equations – Analytic functions – Properties – Harmonic functions – Finding harmonic conjugate – Conformal mapping (w=z+a, w= az, w=1/z,) – Mobius transformation and their properties.

Complex Variables I (Integration)

Cauchy Integral formula – Cauchy Integral theorem – Taylor's series – Singularities of analytic functions – Laurent's series.

Module II **22 Hours**

Complex Variables II (Integration)

Residues – Cauchy Residue theorem – Contour integrals – Evaluation of real definite integrals around unit circle and semi-circle (Excluding poles on the real axis).

Laplace Transform

Laplace Transform – Properties of Laplace Transform – Laplace transform of derivatives and integrals – Laplace transform of periodic functions -Inverse Laplace transforms - Convolution theorem – Solution of ordinary differential equations by Laplace Transform method.

Fourier Series

Dirichlet's condition -Fourier series – Even and odd functions- Half range sine and cosine series - Parseval's identity--Harmonic Analysis.

List of Experiments: **30 Hours**

1. Find gradient of a given scalar function, divergence, and curl of a vector function.
2. Verify Green's theorem in a plane.
3. Graphically plot time and frequency domain of standard functions and compute Laplace transform of In- built functions.
4. Find the Fourier series of a periodic function.
5. Compute Inverse Laplace transform of In- built functions.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Explain the concepts of Vector Differentiation and Integration.	Apply
CO2: Using the concept of complex variables to construct analytical functions and evaluate definite integrals.	Apply
CO3: Apply Laplace transform techniques to solve ordinary differential equations.	Apply
CO4: Compute the Fourier series expansion for given periodic functions.	Apply
CO5: Develop programs using Complex Variables and Transforms concepts through modern tool.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	2	-	-	-	-	-	-	-	-	-	-	-	-
CO3	3	2	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	2	-	-	-	-	-	-	-	-	-	-	-	-
CO5	-	-	-	-	3	-	-	-	-	-	-	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Erwinkreyzig, Advanced Engineering Mathematics, 10th edition, John Wiley& Sons, 2011.

T2. Veerarajan T., Engineering Mathematics for first year, 3rd edition, Tata McGraw-Hill, New Delhi, 2019.

Reference Book(s):

R1. G.B.Thomas and R.L Finney, Calculus and Analytic Geometry, 9th edition, Pearson, Reprint, 2002.

R2. B.S.Grewal, Higher Engineering Mathematics, Khanna Publishers, 36th Edition, 2010.

R3. P. Sivaramakrishna Das , C. Vijayakumari , Engineering Mathematics, Pearson India, 2017.

Web References:

1. https://nptel.ac.in/courses/111107112
2. https://nptel.ac.in/courses/111104031

Course Code: 23CHI202		Course Title: Chemistry for Electronics Engineering	
Course Category: Minor		Course Level: Introductory	
L:T:P (Hours/Week) 3: 0:2	Credits:4	Total Contact Hours:75	Max Marks:100

Course Objectives

The course is intended to impart the knowledge of chemistry involved in Electrochemistry and Batteries, Lithium-ion battery, Corrosion and its control, Spectroscopic technique, E – Waste Management and Nanomaterials.

Module I **23 Hours**

Battery Chemistry: Basic working principle and terminologies in Battery Chemistry - Oxidation and reduction - types of batteries -Characteristics of batteries – Lead Acid battery. Fuel cells: Construction, working and applications – Hydrogen Oxygen fuel cell.

Lithium-ion battery: Introduction-Components of lithium battery, types - (LFP-NMC-NCA-LMO- LCO-LTO) and characteristics- Comparison of different types of Lithium battery. Applications of Lithium-ion battery in mobile electronics.

Corrosion and its Control: Corrosion – Dry and wet corrosion – Galvanic corrosion and Concentration cell corrosion - Factors influencing corrosion. Corrosion Control methods – Cathodic protection methods, Metallic coating – Galvanizing, Tinning – Chrome plating and Electroless plating of Nickel

Module II **22 Hours**

Analytical Techniques: Spectroscopy- Electromagnetic spectrum, Absorption and Emission spectroscopy – Relationship between absorbance and concentration – Derivation of Beer-Lambert's law. UV - Visible Spectroscopy, Atomic Absorption Spectroscopy and Flame Photometry

Electronic Waste Management: Introduction- Concepts of e-waste management. Global context in e- waste; E-waste pollutants and hazardous properties, Effects of pollutant (E-waste) on human health and environment. E – Waste Management - Technology of disposal and Recovery of materials (Landfilling, Acid Bath, Incineration, Recycling and Reuse). Status of E-waste management in India.

Nanomaterials: Introduction - Difference between bulk and nanomaterials - Size dependent properties. Types of nano scale materials: Particles, clusters, rods, and tubes. Applications of nanomaterials.

List of Experiments: **30 Hours**

1. Estimation of Fe2+ by potentiometric titration.
2. Determination of corrosion rate by weight loss method.
3. Estimation of iron in water by spectrophotometry
4. Green Synthesis of Silver Nanoparticles by Neem leaf.
5. Conductometric titration of strong acid against strong base.
6. Determination of strength of acid by pH metry.
7. Performance analysis of battery.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Understand and explain the chemistry involved in Electrochemistry, Batteries, Corrosion, Spectroscopic techniques, E-waste management and Nanomaterials.	Understand
CO2: Apply the acquired knowledge of chemistry to solve the Engineering and environmental problems.	Apply
CO3: Apply the engineering problems through the concept of Electro chemistry, Batteries, Spectroscopic techniques, E-waste techniques and Nanomaterials.	Apply
CO4: Apply the knowledge of chemistry to investigate Engineering materials by volumetric and instrumental methods and analyze, interpret the data to assess, and address the issues of Environmental Pollution.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	-	-	-	3	-	-	-	-	-	-	-	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Jain and Jain, “Engineering Chemistry”, 17th Edition, Dhanpat Rai Publishing Company, New Delhi, 2018.

T2. Wiley “Engineering Chemistry”, 2nd Edition, Wiley India Pvt Ltd, New Delhi, 2011.

T3. Hester R.E., and Harrison R.M, “Electronic Waste Management”, Science, 2009

Reference Book(s) :

R1. Dara S. S and Umare S. S., "A textbook of Engineering Chemistry", 12th edition, S. Chand & Co Ltd, New Delhi , 2014.

R2. V. R. Gowariker, N. V. Viswanathan and Jayadev Sreedhar, "Polymer Science",4th edition New Age International(P) Ltd, Chennai ,2021.

R3. Jeffery G. H., Bassett. J., Mendham J and Denny R. C., Vogel's "Textbook of Quantitative Chemical Analysis", 5th edition Oxford, ELBS, London, 2012.

R4. Fowler B, "Electronic Waste" – 1st edition (Toxicology and Public Health Issues), Elsevier, 2017

Web References:

1. http://nptel.ac.in/courses/122101001/downloads/lec.23.pdf
2. https://nptel.ac.in/courses/104106075/Week1/MODULE%201.pdf
3. https://nptel.ac.in/courses/103102015/

Course Code: 23ITT202		Course Title: Problem solving and Python Programming (Common to EA, EC & EV)	
Course Category: Multidisciplinary		Course Level: Introductory	
L: T:P (Hours/Week) 3: 0:0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The objective of the course is to introduce learners to the fundamentals of programming using the Python language. The course aims to equip participants with the necessary skills and knowledge to write efficient, readable, and maintainable Python code.

Module I **23 Hours**

Basics of Python: Features - Variables and Data Types - Expressions and Statements - Operators.

Control Flow: Conditional Statements – Looping and Iterative Statements

Functions and File Handling: Introduction to Functions - Recursive Functions - Introduction to Files and File Handling

Data Structures in Python: Lists: Functions and Methods - Tuples: Operations and Built-in Functions - Sets: Functions and Methods - Dictionaries: Functions and Methods - Strings: Operators and Built-In String Functions

OOP Concepts: Classes and Objects: Modifiers in Classes - Method Invocation in Classes - Inheritance and Polymorphism.

Module II **22 Hours**

Exception Handling: Errors and Exceptions

GUI Programming with TKinter: GUI Basics - Working with the TKinter Library

Widgets and Events: Adding Widgets and Binding Events - Message and Entry Widgets - Checkboxes and Radio Buttons - Menus and Lists - Canvas for Drawing

Data Visualization with Matplotlib: Introduction to Matplotlib Library - Line and Bar Plots - Scatter Plots - Pie Charts - Working with Multiple Figures - 3D Plots - Plotting Using Files.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply Python programming constructs and data structure techniques to solve practical problems and build functional applications.	Apply
CO2: Categorize the OOPs concepts to create modular and extensible Python programs.	Analyze
CO3: Infer the errors and exceptions in Python programs using exception handling techniques to ensure robust and fault-tolerant code	Analyze

CO4: Build graphical user interfaces (GUIs) using TKinter, effectively incorporating various widgets and event binding to create interactive and visually appealing applications	Apply
CO5: Employ the Matplotlib library for data visualization to present data and insights in a visually impactful method	Apply
CO6: Combine the Python language features and libraries to provide solutions collaboratively with Ethical values to the practical problems	Create

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-	-	3
CO3	-	3	-	-	-	-	-	-	-	-	-	-	-	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	-
CO5	3	-	-	-	-	-	-	-	-	-	-	-	3	-
CO6	-	-	3	2	2	-	-	3	3	3	3	3	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Peter Wentworth, Jeffrey Elkner, Allen B. Downey, and Chris Meyers, "How to Think Like a Computer Scientist: Learning with Python",3rd Edition, O'Reilly, 2020.

T2. Mark Lutz, "Powerful Object-Oriented Programming Python", 4th Edition, O'Reilly, 2013.

Reference Book(s):

R1. Mark Lutz, "Learning Python, Powerful OOPs", 5th Edition, O'Reilly, 2013.

R2. Zelle, John M, "Python Programming: An Introduction to Computer Science", Franklin Beedle& Associates, 2003.

Web References:

1. https://docs.python.org/3/tutorial/
2. https://www.learnpython.org/
3. https://www.pyschools.com/
4. https://archive.nptel.ac.in/courses/106/106/106106182/

Course Code: 23MEL001		Course Title: ENGINEERING DRAWING (Common to AD,AM,AU,CS,EA ,EC,EE,EV,IT,ME, SC)	
Course Category: Multidisciplinary		Course Level: Introductory	
L:T:P(Hours/Week) 1: 0: 3	Credits:2.5	Total Contact Hours: 60	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on basic dimensioning. 2D and 3 D drawings such as points, lines, planes, and solids on first quadrant.

Module I **22 Hours**

Basics of Engineering Drawing: Importance of graphics in engineering applications – Use of drafting instruments – BIS conventions and specifications – Size, layout and folding of drawing sheets – Lettering and dimensioning. Basic Geometrical constructions –Orthographic projection- Free hand Sketching.

Projection of Points, Lines: First angle projection-projection of points. Projection of straight lines (only First angle projections) inclined to both the principal planes - Determination of true lengths and true inclinations by rotating line method and traces by rotating object method.

Projection of Solids: Projection of simple solids like prisms, pyramids, cylinder and cone when the axis is inclined to one of the principal planes by rotating object method. Practicing three dimensional modeling of simple objects by CAD Software (Not for examination).

Module II **23 Hours**

Sectioned Solids: Sectioning of simple solids like prisms, pyramids, cylinder and cone when the axis is inclined to one reference plane by cutting planes inclined to one reference plane and perpendicular to the other – Orthographic views of sections of simple solids.

Development of Surfaces: Development of lateral surfaces of simple and truncated solids – Prisms, pyramids, cylinders using straight line and radial line method.

List of Experiments **45 Hours**

1. Lettering & Dimensioning
2. Projection of Points & Lines
3. Orthographic projections
4. Projection of Simple Solids
5. Projection of Section of Simple Solids
6. Development of Surfaces
7. Isometric Projections

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the concepts related to free hand sketching, orthographic and Isometric projection in first quadrant.	Understand
CO2: Apply the concepts and draw projections of points in four different quadrants and lines located first quadrant.	Apply
CO3: Apply the concepts and draw projections and sections of simple solids using Rotating object method.	Apply
CO4: Apply the concepts and draw lateral surface of simple solids using straight line and radial line development methods.	Apply
CO5: Apply the concepts and draw isometric view of simple solids and truncated solids using principles of isometric projection.	Apply
CO6: Conduct experiments to demonstrate concepts, implement and analyze the drawing concepts using engineering tool : Using AutoCAD.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO5	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO6	-	3	-	-	3	-	-	-	1	1	-	1	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Cencil Jensen, Jay D.Helsel and Dennis R. Short, " Engineering Drawing and Design", Tata McGraw Hill India, New Delhi, 3rd edition, 2019.

Reference Book(s):

R1. Basant Agarwal and Agarwal C.M., "Engineering Drawing", Tata McGraw Hill India,New Delhi, 2nd edition, 2014.

R2. Dhananjay A. Jolhe, "Engineering Drawing with an introduction to AutoCAD" Tata McGraw India, New Delhi, 3rd edition, 2010.

R3. Bhatt N.D. and Panchal V.M., "Engineering Drawing", Charotar Publishing House, Gujarat, 54rd edition, 2023.

PUBLICATIONS OF BUREAU OF INDIAN STANDARDS

1. IS 10711 – 2001: Technical products Documentation – Size and lay out of drawing sheets.IS 9609 (Parts 0 & 1) – 2001: Technical products Documentation – Lettering.
2. IS 10714 (Part 20) – 2001 & SP 46 – 2003: Lines for technical drawings.IS 11669 – 1986 & SP 46 – 2003: Dimensioning of Technical Drawings.
3. IS 15021 (Parts 1 to 4) – 2001: Technical drawings – Projection Methods. The mode of delivery is like practical.

Web References:

1 http://nptel.ac.in/courses/112103019/

2 https://www.coursera.org/specializations/autodesk-cad-cam-cae-mechanical-engineering

Course Code: 23ESL201		Course Title: Professional Skills 1: Problem solving skills & Logical Thinking 1 (Common to all B.E/B.Tech Programmes)	
Course Category: SEC		Course Level: Introductory	
L:T:P(Hours/Week) 0: 0: 2	Credits: 1	Total Contact Hours:30	Max Marks:100

Course Objectives:

To enhance the students' numerical, analytical, and logical reasoning ability.

To make them prepare for various public and private sector exams and placement drives.

Module I Quantitative Ability 20 Hours

Number System and LCM & HCF- Percentage- Ratio and Proportion - Average- Progressions- Ages-Partnership- Mixture & Allegation - Profit and loss- Interest calculation- Data interpretation.

Module II Reasoning Ability 10 Hours

Seating Arrangement- Linear, circular and Complex – Direction Problems- Blood Relation- Puzzles- Crypt arithmetic- Venn diagrams- Statement and conclusion- Statement and argument- Causes and effects- Self-Learning.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Build the competence in numerical, analytical, and logical reasoning ability	**Apply**

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	3	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1: Dr. R. S. Aggarwal. "Quantitative Aptitude for Competitive Examinations" Sultan Chand & Sons Pvt. Ltd, New Delhi, 2018.

T2: Dr. R. S. Aggarwal. "A Modern Approach to Logical Reasoning", Sultan Chand & Sons Pvt. Ltd, New Delhi, 2018

Reference Book(s):

R1: R. V. Praveen. "Quantitative Aptitude and Reasoning" 2nd Revised Edition, Prentice-Hall of India Pvt.Ltd, 2013

R2: Arun Sharma. "Quantitative Aptitude for Common Aptitude Test", McGraw Hill Publications, 5th Edition, 2020

R3: Arun Sharma. "Logical Reasoning for Common Aptitude Test", McGraw Hill Publications, 6th Edition, 2021.

Web References:

1. https://www.indiabix.com/aptitude/questions-and-answers/
2. https://www.geeksforgeeks.org/aptitude-questions-and-answers/

Course Code: 23VAT201		Course Title: TAMILS AND TECHNOLOGY (Common to all B.E/B.Tech Programmes)	
Course Category: VAC		Course Level: Introductory	
L: T:P (Hours/Week) 1:0:0	Credits: 3	Total Contact Hours: 15	Max Marks: 100

Pre-requisites: NIL

Course Objectives:

மாணவர்கள் இப்பாடத்தை கற்றலின் மூலம்

CO.1 நெசவு மற்றும் பானைத் தொழில்நுட்பம், வடிவமைப்பு மற்றும் கட்டிடத் தொழில்நுட்பம், உற்பத்தித் தொழில்நுட்பம், வேளாண்மை மற்றும் நீர்ப்பாசனத் தொழில்நுட்பம் ஆகியன குறித்து அறிந்து கொள்ள இயலும்.

CO.2 அறிவியல் தமிழ் மற்றும் கணினித் தமிழ் குறித்து அறிந்து கொள்ள இயலும்.

தமிழரும் தொழில்நுட்பமும்

அலகு 1 - நெசவு மற்றும் பானைத் தொழில்நுட்பம் **3 Hours**

சங்க காலத்தில் நெசவுத் தொழில் - பானைத் தொழில்நுட்பம் - கருப்பு சிவப்பு பாண்டங்கள் - பாண்டங்களில் கீறல் குறியீடுகள்

அலகு 2 - வடிவமைப்பு மற்றும் கட்டிடத் தொழில்நுட்பம் **3 Hours**

சங்க காலத்தில் வடிவமைப்பு மற்றும் கட்டுமானங்கள் ஷ சங்க காலத்தில் வீட்டுப் பொருட்களில் வடிவமைப்பு சங்க காலத்தில் கட்டுமானப் பொருட்களும் நடுகல்லும் - சிலப்பதிகாரத்தில் மேடை அமைப்பு பற்றிய விவரங்கள் - மாமல்லபுரச் சிற்பங்களும், கோவில்களும் - சோழர் காலத்துப் பெருங்கோயில்கள் மற்றும் பிற வழிபாட்டுத் தலங்கள் - நாயக்கர் காலக் கோயில்கள் - மாதிரி கட்டமைப்புகள் பற்றி அறிதல், மதுரை மீனாட்சி அம்மன் ஆலயம் மற்றும் திருமலை நாயக்கர் மஹால் செட்டிநாட்டு வீடுகள், பிரிட்டிஷ் காலத்தில் சென்னையில் இந்தோ - சாரோசெனிக் கட்டிடக் கலை.

அலகு 3 - உற்பத்தித் தொழில்நுட்பம் **3 Hours**

கப்பல் கட்டும் கலை - உலோகவியல் - இரும்புத் தொழிற்சாலை - இரும்பை உருக்குதல், எஃகு - வரலாற்றுச் சான்றுகளாக செம்பு மற்றும் தங்க நாணயங்கள் - நாணயங்கள் அச்சடித்தல் மணி உருவாக்கும் தொழிற்சாலைகள் - கல்மணிகள், கண்ணாடி மணிகள் - சுடுமண் மணிகள் - சங்கு மணிகள் - எலும்புத் துண்டுகள் - தொல்லியல் சான்றுகள் - சிலப்பதிகாரத்தில் மணிகளின் வகைகள்.

அலகு 4 வேளாண்மை மற்றும் நீர்ப்பாசனத் தொழில்நுட்பம் **3 Hours**

அணை, ஏரி, குளங்கள், மதகு - சோழர்காலக் குமுழித் தூம்பின் முக்கியத்துவம் - கால்நடை பராமரிப்பு - கால்நடைகளுக்காக வடிவமைக்கப்பட்ட கிணறுகள் - வேளாண்மை மற்றும வேளாண்மைச் சார்ந்த செயல்பாடுகள் - கடல்சார் அறிவு - மீன் வளம் - முத்து மற்றும் முத்துக் குளித்தல் - பெருங்கடல் குறித்த பண்டைய அறிவு - அறிவுசார் சமூகம்.

அலகு 5 - இந்திய தேசிய இயக்கம் மற்றும் இந்திய பண்பாட்டிற்குத் தமிழர்களின் பங்களிப்பு **3 Hours**

இந்திய விடுதலைப் போரில் தமிழர்களின் பங்கு இந்தியாவின் பிறபகுதிகளில் தமிழ்ப் பண்பாட்டின் தாக்கம் - சுய மரியாதை இயக்கம் - இந்திய மருத்துவத்தில் சித்த மருத்துவத்தின் பங்கு - கல்வெட்டுகள், கையெழுத்துப் படிகள்- தமிழ்ப் புத்தகங்களின் அச்சு வரலாறு.

Course Outcomes	**Cognitive Level**
மாணவர்கள் இப்பாடத்தை கற்றபின்	
CO1 : நெசவு மற்றும் பானைத் தொழில்நுட்பம், வடிவமைப்பு மற்றும் கட்டிடத் தொழில்நுட்பம், உற்பத்தித் தொழில்நுட்பம், வேளாண்மை மற்றும் நீர்ப்பாசனத் தொழில்நுட்பம் ஆகியன குறித்து அறிந்து கொள்வார்கள்.	அறிதல் (Understand)
CO2: அறிவியல் தமிழ் மற்றும் கணினித் தமிழ் குறித்து அறிந்து கொள்வார்கள்.	அறிதல் (Understand)

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	1	-	-
CO2	-	-	-	-	-	-	-	-	-	-	-	1	-	-

High-3; Medium-2; Low-1

Text Cum Reference Book(s):

1. தமிழக வரலாறு - மக்களும் பண்பாடும் -கே.கே.பிள்ளை (வெளியீடு. தமிழ்நாடு பாடநூல் மற்றும் கல்வியியல் பணிகள் கழகம்)
2. கணினித் தமிழ் - முனைவர் இல. சுந்தரம் (விகடன் பிரசுரம்)
3. கீழடி - வைகை நதிக்கரையில் சங்க கால நகர நாகரிகம் (தொல்லியல் துறை வெளியீடு
4. பொருநை - ஆற்றங்கரை நாகரிகம் (தொல்லியல் துறை வெளியீடு
5. Social Life of Tamils (Dr.K.K.Pillay) A joint publication of TNTB & ESC and RMRL (in print)
6. Social Life of the Tamils - The Classical Period (Dr.S.Singaravelu) (Published by: International Institute of Tamil Studies.
7. Historical Heritage of the Tamils (Dr.S.V.Subatamanian, Dr.K.D. Thirunavukkarasu) (Published by: International Institute of Tamil Studies).
8. The Contributions of the Tamils to Indian Culture (Dr.M.Valarmathi) (Published by: International Institute of Tamil Studies.)
9. Keeladi - 'Sangam City Civilization on the banks of river Vaigai' (Jointly Published by: Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation, Tamil Nadu)
10. Studies in the History of India with Special Reference to Tamil Nadu (Dr.K.K.Pillay) (Published by: The Author)
11. Porunai Civilization (Jointly Published by: Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation, Tamil Nadu)
12. Journey of Civilization Indus to Vaigai (R.Balakrishnan) (Published by: RMRL) - Reference Book.

Course Code: 23CHT202		Course Title: Environmental Sciences (Common to all B.E/B.Tech Programmes)	
Course Category: Multidisciplinary		Course Level: Introductory	
L: T:P (Hours/Week) 1: 0: 0	Credits: Mandatory Non- Credit Course	Total Contact Hours: 15	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on sustainable utilization of natural resources, prevention of pollution, disaster management and environmental issues & public awareness on ecosystem.

Module I **8 Hours**

Natural Resources

Role of individual in conservation of natural resources; Equitable use of resources for sustainable lifestyles.

Environmental Pollution and Disaster Management

Role of an individual in prevention of pollution; Disaster management: floods, earthquake, cyclone, and landslides.

Environmental Ethics and Legislations

Environmental ethics: Environment Protection Act; Air Act; Water Act; Wildlife Protection Act; Forest Conservation Act; Issues involved in enforcement of environmental legislation.

Module II **7 Hours**

Environmental Issues and Public Awareness

Public awareness - Environment and human health.

Environmental Activities

(a) Awareness Activities:

i. Small group meetings about water management, promotion of recycle use, generation of less waste, avoiding electricity waste.
ii. Slogan making event.
iii. Poster making event.

(b) Actual Activities:

i. Plantation.
ii. Cleanliness drive.
iii. Drive for segregation of waste.
iv. To know about the different varieties of plants.
v. Shutting down the fans and ACs of the campus for an hour or so.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Explain the use of natural resources for a sustainable life as an individual in prevention of pollution.	Understand
CO 2: Apply the environmental ethics and legislations for various environmental issues.	Apply
CO 3: Create the public awareness on environment and human health as an individual or team through various activity based learning.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	3	3	-	-	-	-	3	-
CO3	3	-	-	-	-	3	3	-	3	3	-	-	3	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Benny Joseph, “Environmental Studies", Tata McGraw Hill, New Delhi, 2006.

T2. Mackenzie Davis and Susan Masten, “Principles of environmental engineering and science”, Mc-Graw Hill, 3rd Edition, 2014.

Reference Book(s):

R1. Trivedi R.K. “Handbook of Environmental Laws, Rules, Guidelines, Compliances and Standards", Vol.I and II, Enviro Media.

R2. Cunningham, W.P.Cooper, T.H. Gorhani, “Environmental Encyclopedia", Jaico Publishing House, Mumbai, 2001.

Web References:

1. https://onlinecourses.nptel.ac.in/noc23_hs155/preview.
2. https://en.wikipedia.org/wiki/Environmental_science

Passed in 2nd Board of Studies Meeting held on 11.01.2024
Approved in 18th Academic Council Meeting held on 23.03.2024 BoS Chairman

SEMESTER III

Course Code: 23MAI301		Course Title: Numerical Techniques and Linear Algebra	
Course Category: Minor		Course Level: Intermediate	
L: T:P (Hours/Week) 3:0:2	Credits: 4	Total Contact Hours: 75	Max Marks:100

Course Objectives:

This course is designed to give an overview of numerical methods and provide knowledge and skills needed to apply these tools and techniques for decision making in various fields of science and engineering.

Module I **23 Hours**

Solution of System of Linear Equations and Eigenvalue

Solution of system of linear equations– Direct methods: Gaussian elimination method – Indirect methods: Gauss Jacobi method, Gauss-Seidel method– sufficient conditions for convergence –Solution of nonlinear equations: Newton Raphson method – Power method to find the dominant Eigen value and the corresponding Eigen vector – Application of Eigen value and the corresponding Eigen vector.

Interpolation, Numerical Differentiation, and Integration: Interpolation – Newton's forward, backward interpolation – Lagrange's interpolation. Numerical Differentiation and Integration – Trapezoidal rule – Simpson's 1/3 rule – Double integration using Trapezoidal rule.

Numerical Solution of Ordinary Differential Equation: Numerical solution of first order ordinary differential equation-Single step method: Taylor's series- Euler's method – Runge-Kutta method of fourth order – Multi step method: Milne's predictor corrector methods for solving first order differential equations.

Module II **22 Hours**

Vector Spaces: Vector spaces- Subspace of a vector space- basis and dimension of vector space – linear combination and spanning sets of vectors – linear independence and linear dependence of vectors – Row space, Column space and Null space – Rank and nullity of subspaces.

Orthogonality and Inner Product Spaces: Inner product of vectors: length of a vector, distance between two vectors, and orthogonality of vectors – Orthogonal projection of a vector – Gram-Schmidt process to produce orthogonal and orthonormal basis – Inner product spaces.

List of Experiments: **30 Hours**

1. Use python to solve system of linear equations using Gauss elimination method.
2. Use python to solve algebraic and transcendental equation by Newton Raphson method.
3. Use python to interpolate using Newton's forward and backward interpolation method.
4. Use python to solve first order ordinary differential equation using Range kutta method of 4^{th} order.

   Use python to find the basis of row space, column space and null space of a given matrix.
5. Use python to compute the inner product of two vectors and to check whether the given vectors are orthogonal.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Solve the system of linear equations, nonlinear equations & calculate the dominant Eigen value	Apply
CO2: Determine the unknown values from the given set of data & Compute derivatives and integrals.	Apply
CO3: Solve first order ordinary differential equation using Numerical Techniques.	Apply
CO4: Apply the concept of vector spaces and inner product spaces to produce orthogonal and orthonormal basis.	Apply
CO5: Apply the concepts of Numerical techniques and Linear Algebra to electrical and electronics engineering.	Apply
CO6: Apply the concepts of Numerical techniques using modern tools and report the result and inference. (For laboratory content only)	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	1	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	1	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	1	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	1	-	-
CO5	2	-	-	-	-	-	-	-	-	1	-	1	-	-
CO6:	3	-	-	-	3	-	-	-	1	-	-	1	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Grewal, B.S. and Grewal, J. S., "Numerical Methods in Engineering and Science",11^{th} Edition, Khanna Publishers, New Delhi, 2013.

T2. Curtis F. Gerald, Patric.O. *W*heatley, "Applied Numerical Analysis", 7^{th} Edition, Pearson Education, Asia, New Delhi, 2009.

Reference Book(s):

R1. Steven Chopra, Raymond.P. Canale, “Numerical Methods for Engineers”, 7th Edition, 2015.

R2. Jain M.K, Iyengar.S.R. K and Jain.R. K, “Numerical Methods for Scientific and Engineering Computation”, 6th Edition, New Age Publishers, 2012.

R3. Gilbert Strang, “Linear algebra and its applications”, 4th Edition, Cengage Learning(RS), 2012.

Web References:

1. http://nptel.ac.in/courses/122104018/node2.html
2. http://nptel.ac.in/courses/111105038

Course Code: 23EVT301		Course Title: Circuit Theory and Network Analysis	
Course Category: Major		Course Level: Intermediate	
L: T:P (Hours/Week) 3: 0:0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to explain the application of the nodal and mesh analysis to solve the circuit parameters, resonance in coupled circuits. Additionally, the course explains to utilize Network theorems for analysis and synthesis two port networks.

Module I **23 Hours**

DC CIRCUIT ANALYSIS: Basic Components of electric Circuits, Charge, current, Voltage and Power, Voltage and Current sources, Ohms Law, Kirchhoff's Current Law, Kirchhoff's voltage law, The single Node – Pair Circuit, series and Parallel Connected Independent Sources, Resistors in Series and Parallel, voltage and current division, Nodal analysis, Mesh analysis.

NETWORK THEOREM AND DUALITY: Useful Circuit Analysis techniques - Linearity and superposition, Thevenin and Norton Equivalent Circuits, Maximum Power Transfer, Delta-Wye Conversion, Duals, Dual circuits, Analysis using dependent current sources and voltage sources

Module II **22 Hours**

Network analysis: Sinusoidal Steady State analysis, Characteristics of Sinusoids, The Complex Forcing Function, The Phasor, Phasor relationship for R, L, and C, impedance and Admittance, Nodal and Mesh Analysis, Phasor Diagrams, AC Circuit Power Analysis, Instantaneous Power, Average Power, apparent Power and Power Factor, Complex Power.

TRANSIENTS IN RLC CIRCUITS: Basic RL and RC Circuits, The Source- Free RL Circuit, The Source-Free RC Circuit, The Unit- Step Function, Driven RL Circuits, Driven RC Circuits, RLC Circuits

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply Kirchhoff's and Ohm's Laws to determine electrical parameters in DC resistive circuits.	Apply
CO2: Utilize network theorems to simplify and Analyze complex DC circuits.	Apply
CO 3: Compute AC circuit parameters using Nodal and Mesh analysis with phasors.	Apply
CO 4: Interpret transient responses of RL, RC, and RLC circuits.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	-	3	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Hayt Jack Kemmerly, Steven Durbin, "Engineering Circuit Analysis", Mc Graw Hill education, 9th Edition, 2018.

T2. Charles K, Alexander & Mathew N.O.Sadiku, "Fundamentals of Electric Circuits", Mc Graw-Hill, 2nd Edition, 2003.

T3. Joseph Edminister and Mahmood Nahvi, —Electric Circuits, Schaum's Outline Series, Tata McGraw Hill Publishing Company, New Delhi, Fifth Edition Reprint 2016.

Reference Book(s):

R1. Robert.L. Boylestead, "Introductory Circuit Analysis", Pearson Education India, 12th Edition,

R2. David Bell, "Fundamentals of Electric Circuits", Oxford University press, 7th Edition, 2009.

R3. Allan H,Robbins, Wilhelm C.Miller, “Circuit Analysis Theory and Practice", Cengage Learning, Fifth Edition, 1st Indian Reprint 2013

Web References:

1. https://nptel.ac.in/courses/108106075

Course Code: 23EVT302		Course Title: Analog Electronics	
Course Category: Major		Course Level: Intermediate	
L: T:P (Hours/Week) 3: 0:0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on design and analysis of amplifier and oscillator circuits using BJTs and MOSFETs.

Module I **23 Hours**

Biasing: DC Loadline, operating point, Various biasing methods for BJT-Design-Stability-Bias compensation, Thermal stability, DC bias analysis of MOSFET circuits. **Feedback Amplifiers and Stability:** Basic feedback concepts – Properties of Negative feedback – Feedback topologies– Analysis of feedback amplifiers – stability analysis on amplifier – Gain and Phase-margins- Frequency compensation. **Discrete BJT Amplifiers:** Small signal Analysis of Common Emitter-AC Loadline, Voltage swing limitations, Common Collector, and common base amplifiers – Differential amplifiers- CMRR- Darlington Amplifier- Multi stage amplifiers-Cascode Amplifier.

Module II **22 Hours**

MOSFET: Small signal Analysis of amplifiers- Common source amplifier, Voltage swing limitations, small signal analysis of Source follower and Common Gate amplifiers, Cascode amplifiers, Differential amplifiers **Frequency Analysis**: Short circuit current gain, cutoff frequency–fα, fβ of BJT, Unity Gain Bandwidth of BJT and MOSFET, Low frequency analysis, Miller effect, High frequency analysis of single stage BJT and MOSFET amplifiers.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Construct BJT and MOSFET biasing circuits with appropriate techniques to ensure thermal and operating point stability.	Apply
CO 2: Demonstrate the performance and stability of feedback amplifiers using gain and phase margins.	Apply
CO 3: Examine small-signal MOSFET amplifiers to determine gain and signal swing.	Analyze
CO 4: Develop the frequency response of BJT and MOSFET amplifiers at low and high frequencies.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Donald .A. Neamen, "Micro Electronics: Circuit Analysis and Design", 4th Edition, Tata McGraw Hill, 2021.

T2. Adel.S.Sedra, Kenneth C.Smith, "Micro Electronic Circuits: Theory and Applications",7th Edition,Oxford University Press,2017

Reference Book(s):

R1. Behzad Razavi,"Design of Analog CMOS Integrated Circuits",Tata McGraw Hill,2017.

R2. Paul Gray, Hurst, Lewis, Meyer, "Analysis and Design of Analog Integrated Circuits", John Willey & Sons, 5th Edition,2009.

R4. Paul Horowitz, Winfield Hill, “The Art of Electronis”,Cambridge University Press, 3rd Edition,2015(Reference for Lab)

Web References:

1. https://archive.nptel.ac.in/courses/108/105/108105158/

Course Code: 23EVT303		Course Title: Digital Electronics	
Course Category: Major		Course Level: Intermediate	
L: T:P (Hours/Week) 3: 0:0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to teach Boolean laws, simplification techniques and implement the same to design combinational, synchronous, and asynchronous sequential circuits. Moreover, the course imparts a knowledge on the design of various memory devices, shift registers.

Module I **22 Hours**

Review of number systems – Representation - Conversions, Review of Boolean algebra - Theorems, Canonical forms, and Standard forms -Implementation of Boolean expressions using universal gates, Simplification of Boolean expressions, Karnaugh map, Tabulation methods.

Combinational Circuits: Code-Converters, Half and Full Adders, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Magnitude Comparator, Decoder, Encoder, Priority Encoder, Multiplexer, Demultiplexer.

Module II **23 Hours**

Synchronous Sequential Circuits: Latches, Flip flops – SR, JK, T, D, Master/Slave FF, Triggering of FF, Analysis, and design of clocked sequential circuits – Design - Moore/Mealy models, State minimization, State assignment, Counters, Ripple Counters, Ring Counters, Shift registers, Universal Shift Register. Use cases **Asynchronous Sequential Circuits:** Analysis - Stable and unstable states, Cycles and races, Design of Fundamental mode sequential circuits - State reduction, Race free assignments, Hazards and its types, Design of Hazard free circuits. Use cases.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Utilize logic minimization techniques to simplify Boolean expressions.	Apply
CO 2: Develop the combinational circuits using logic gates implementing Boolean simplification.	Apply
CO 3: Construct synchronous sequential circuits using flip-flops, counters, and state machines (Moore/Mealy models) to meet given design specifications.	Apply
CO 4: Construct stable asynchronous sequential circuits using hazard-free design techniques.	Apply
CO5: Apply the basic digital concepts in real world application and present a case study. (only for Assignment)	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	-	-	3	-	-	-	-	-	-	-	-	-	1	1
CO4	-	-	3	-	-	-	-	-	-	-	-	-	1	1
CO5	3	-	-	-	1	-	-	-	1	1	-	1	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. M. Morris Mano and Michael D. Ciletti, 'Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog, 6e', Pearson, 6th Edition, 2018.

T2. Charles H. Roth, Jr. and Larry L. Kinney, 'Fundamentals of Logic Design', Cengage Learning, 7th Edition, 2014.

Reference Book(s):

R1. William I. Fletcher, "An Engineering Approach to Digital Design - softcover", Prentice- Hall of India, 2015.

R2. Floyd T.L., "Digital Fundamentals", 11th Edition by Pearson Education, 2020

R3. John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 5th Edition, 2018.

R4. John M.Yarbrough, "Digital Logic Application & Design", Thomson, 2010.

R5. Donald D.Givone, "Digital Principles and Design", TMH, 2003.

Web References:

1. https://nptel.ac.in/courses/117105080/
2. 2. https://nptel.ac.in/courses/117106086/

Course Code: 23EVI301		Course Title: Data Structures and Algorithms using Python	
Course Category: Multi-Disciplinary		Course Level: Intermediate	
L: T:P (Hours/Week) 2:0:2	Credits: 3	Total Contact Hours: 60	Max Marks:100

Course Objectives:

The course is intended to teach students to create and implement required linear and non-linear data structures for given applications. Also, the course is intended to provide ability to apply suitable searching and sorting techniques to solve a given problem.

Module I **16 Hours**

Linear Data structure: Data Structures types - Abstract Data Types - List ADT: Array and Linked List Implementation - Stack ADT: Implementation of Stack – Queue ADT: Implementation of Queue. **Non-Linear Data Structure:** Tree **-** Preliminaries - Binary tree - Tree traversal - Applications - Binary search tree. **Data Structures for Switching Functions:** Binary Decision trees - Introduction to Ordered Binary decision trees (OBDD) - Boolean functions - Boolean algebra - Switching functions - Subfunctions and Shannon's expansion - Visual representation.

Module II **14 Hours**

Non Linear Data Structure: Graph Representation - Graph Traversals: Depth first and Breadth first traversal - Topological sort - Shortest path algorithms: Weighted Graphs - Dijkstra's algorithms - Minimum Spanning Tree: Prim's and Kruskal's algorithms. **Searching:** Linear Search – Binary Search. **Sorting:** Bubble sort- Insertion Sort - Merge sort –Quick Sort.

List of Experiments: **30 Hours**

1. Implementation of stack and queue
2. Implementation of linked list
3. Applications of stack
   a. Infix to post fix conversion
   b. Evaluation of postfix expression
4. Implementation of Binary search tree
5. Implementation of searching - linear, Binary
6. Implementation of sorting technologies, Merge and Quick sort

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Identify the appropriate data structures as per the specified problem definition using Python.	Apply
CO 2: Develop Tree data structure for the given Scenario.	Apply
CO 3: Develop graph data structure for the given application.	Apply
CO 4: Demonstrate searching and sorting techniques for any given problem with an oral presentation.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	2	-	-	-	-	-	-	-	-	-
CO2	-	-	3	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-	-	-
CO4	-	2	-	-	-	-	-	-	2	2	-	-	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1.Michael T. Goodrich, Roberto Tamassia, Michael H. Goldwasser, “Data Structures and Algorithms in Python”, Wiley, July 2021.

T2.Christoph Meinel and Thorsten Theobald, “Algorithms and Data Structures in VLSI Design”, Springer 1998.

Reference Book(s):

R1. John Canning, Alan Broder, Robert Lafore, “Data Structures & Algorithms in Python”, Addison-Wesley Professional, October 2022.

R2. Dr. Basant Agarwal, “Hands-On Data Structures and Algorithms with Python”, Packt Publishing, July 2022.

R3. Mark Allen Weiss, “Data Structures and Algorithm Analysis in C”, 2nd Edition, Pearson Education Asia, New Delhi, 2011.

Web References:

1. https://www.udemy.com/course/data-structures-and-algorithms-bootcamp-in-python/
2. https://www.udemy.com/course/data-structures-using-python/
3. 3. https://onlinecourses.nptel.ac.in/noc24_cs78/

Course Code: 23EVL301		Course Title: Analog Electronics Laboratory	
Course Category: Major		Course Level: Intermediate	
L:T:P(Hours/Week) 0:0:3	Credits:1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on design and analysis of amplifier and oscillator circuits with using BJTs and MOSFETs.

List of Experiments: **45 Hours**

1. Design and Biasing of BJT using DC Load Line Analysis
2. DC Biasing and Stability Analysis of MOSFET Amplifier
3. Small Signal Analysis of Common Emitter Amplifier
4. Small Signal Analysis of Common Source MOSFET Amplifier
5. Analysis of Feedback Amplifier Using Negative Feedback Topologies
6. Frequency Response of Single Stage BJT Amplifier
7. Frequency Response of Single Stage MOSFET Amplifier
8. Design and Analysis of Differential Amplifier (BJT or MOSFET)
9. Design and Analysis of Cascode Amplifier using BJT
10. Design and Analysis of Source Follower / Common Collector Buffer Amplifier

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Analyze the biasing techniques and small-signal behaviour of BJT and MOSFET amplifier circuits through practical implementation and performance evaluation.	Analyze
CO2: Design and evaluate single-stage and multistage amplifier configurations, including differential, feedback, and Cascode amplifiers, for desired gain, bandwidth, and stability.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	1	1	1	1	1	1
CO2	-	-	3	-	-	-	-	-	1	1	1	1	1	1

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code: 23EVL302		Course Title: Digital Electronics Laboratory	
Course Category: Major		Course Level: Intermediate	
L:T:P(Hours/Week) 0:0:3	Credits:1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to explain the design principles of combinational and sequential circuits.

List of Experiments: **45 Hours**

1. Investigate the logic functions of logic, universal gates and verify the Boolean theorems.
2. Design and Implementation of code converters using logic gates.
3. Design and Implementation of full adder / full subtractor using logic gates.
4. Design and Implementation of encoder / decoder using logic gates.
5. Design and Implementation of multiplexer logic gates.
6. Design and verification of flip-flops.
7. Design and implementation of shift registers using flip flops.
8. Design and implementation of 3-bit synchronous counter, using flip flops and logic gates.
9. Design and implementation of up/down counter, using flip flops and logic gates.
10. Realize state table, state diagram, circuit diagram of mod-5 counter, and implement the same using flip flops and logic gates

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Design combinational circuits using basic gates	Apply
CO2: Build synchronous sequential circuits using Flip Flops.	Apply
CO3: Design shift registers and counters using Flip Flops.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	1	1	1	-	1	1
CO2	3	-	-	-	-	-	-	-	1	1	1	-	1	1
CO3	3	-	-	-	-	-	-	-	1	1	1	-	1	1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code: 23ESL301		Course Title: Professional Skills 2: Problem solving skills & Logical Thinking 2 (Common to all B.E/B.Tech Programmes)	
Course Category: SEC		Course Level: Intermediate	
L: T:P (Hours/Week) 0: 0: 2	Credits: 1	Total Contact Hours:30	Max Marks:100

Course Objectives:

The course is intended to enhance the students' numerical, analytical, and logical reasoning ability. Also, course focus to make learners prepare for various public and private sector exams and placement drives.

Module I **20 Hours**

Quantitative Ability

Time and work –Pipes and cisterns- - Time Speed Distance-Problems on Trains-Boats and Streams- Permutation and Combination-Probability, Mensuration- Heights and distance- Logarithms- Clocks and Calendars – Data Sufficiency

Module II **10 Hours**

Reasoning Ability

Number & Alpha series- odd man out-Coding and Decoding-Syllogisms- - Problems on Cubes and Dices- Logical Venn diagram -Visual Reasoning- Element & logical series.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Enhance their problem solving skills & Logical thinking Skills	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	3	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1: Dr. R. S. Aggarwal. "Quantitative Aptitude for Competitive Examinations" Sultan Chand & Sons Pvt. Ltd, New Delhi, 2018.

T2: Dr. R. S. Aggarwal. "A Modern Approach to Logical Reasoning", Sultan Chand & Sons Pvt. Ltd, New Delhi, 2018

Reference Book(s):

R1: R. V. Praveen. "Quantitative Aptitude and Reasoning" 2nd Revised Edition, Prentice-Hall of India Pvt. Ltd, 2013

R2:Arun Sharma. "Quantitative Aptitude for Common Aptitude Test", McGraw Hill Publications, 5thEdition, 2020

R3:Arun Sharma. "Logical Reasoning for Common Aptitude Test", McGraw Hill Publications, 6thEdition, 2021.

Web References:

1 https://www.indiabix.com/aptitude/questions-and-answers/
2 https://www.geeksforgeeks.org/aptitude-questions-and-answers/
3 https://www.indiabix.com/aptitude/questions-and-answers/
4 https://www.geeksforgeeks.org/aptitude-questions-and-answers/

Course Code: 23VAT301		Course Title: Universal Human Values 2: Understanding Harmony	
Course Category: VAC		Course Level: Introductory	
L: T:P (Hours/Week) 2:1: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Pre-requisites: NIL

Course Objectives:

The course is intended to:

1. Development of a holistic perspective based on self-exploration about themselves (human being), family, society, and nature/existence.
2. Strengthening of self-reflection
3. Understanding (or developing clarity) of the harmony in the human being, family, society, and nature/existence
4. Development of commitment and courage to act
5. Development of a holistic perspective based on self-exploration about themselves (human being), family, society, and nature/existence.

Unit I Introduction to Value Education **9 Hours**

Need for the Value Education; Self -exploration as the process for value education; Continuous Happiness and Prosperity: A look at basic Human Aspirations; Right understanding: Relationship and Physical Facilities; Happiness and Prosperity: current scenario; Method to fulfill the Basic human aspirations

Unit II Harmony in Human Being **9 Hours**

Human being as a co-existence of self (‘I’) and the material ‘Body’; needs of Self ('I') and 'Body'; The Body as an instrument of ‘I’; Harmony in the self (‘I’); Harmony of the self (‘I’) with body; Sanyam and Swasthya; correct appraisal of Physical needs, meaning of Prosperity in detail. Programs to ensure Sanyam and Swasthya

Unit III Harmony in the Family and Society **9 Hours**

Harmony in the Family the basic unit of human interaction; Values in human to human relationship; Trust as the foundational values of relationship; Respect as the right evaluation; Understanding harmony in the society (society being an extension of family); Vision for the universal human order.

Unit IV Harmony in the Nature **9 Hours**

Understanding the harmony in the Nature Interconnectedness, self-regulation and mutual fulfillment among the four orders of nature; Existence as Co-existence at all levels; Holistic perception of harmony in existence.

Unit V Harmony on Professional Ethics **9 Hours**

Natural acceptance of human values; Definitiveness of Ethical Human Conduct; Basic for Humanistic Education, Humanistic Constitution and Humanistic Universal Order; Competence in professional ethics; Case study: holistic technologies, management models and production systems; Strategy for transition towards value-based life and profession.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Reflect on values, aspiration, relationships and hence identify strengths and weaknesses.	Responding
CO2: Appraise physical, mental and social wellbeing of self and practice techniques to promote wellbeing.	Responding
CO3: Value human relationships in family and society and maintain harmonious relationships.	Valuing
CO4: Respect nature and its existence for survival and sustainable of all life forms and hence practice conservation of nature	Valuing
CO5: Appreciate ethical behaviour as a result of value system in personal and professional situations	Receiving

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	1	2	2	-	-	2	-	-
CO2	-	-	-	-	-	1	2	2	2	1	-	2	-	-
CO3	-	-	-	-	-	2	2	2	2	1	-	2	-	-
CO4	-	-	-	-	-	2	2	2	2	-	-	2	-	-
CO5	-	-	-	-	-	1	2	2	2	-	-	2	-	-

High-3; Medium-2; Low-1

Text Book(s):

T1. Human Values and Professional Ethics by R R Gaur, R Sangal, G P Bagaria, Excel Books, NewDelhi, 2010.

Reference Book(s):

R1. Jeevan Vidya: E k Parichaya, A Nagaraj, Jeevan Vidya Prakashan, Amarkantak, 1999.

R2. Human Values, A.N. Tripathi, New Age Intl. Publishers, New Delhi, 2004.

R3. The story of stuff, Annie Leonard, Free Press, New York 2010.

Web References:

1 https://aktu.ac.in/hvpe/ResourceVideo.aspx
2 http://hvpenotes.blogspot.com/
3 https://nptel.ac.in/courses/109/104/109104068/

SEMESTER IV

Course Code: 23MAI401		Course Title: Probability Theory and Statistics	
Course Category: Minor		Course Level: Intermediate	
L: T:P (Hours/Week) 3:0:2	Credits: 4	Total Contact Hours: 75	Max Marks:100

Course Objectives:

The course aims at providing the student to acquire the knowledge on random variables and probability distributions. They gain knowledge regarding hypothesis testing for data.

Module I **23 Hours**

Probability and Random Variables: Axioms of Probability- Conditional Probability- Total Probability -Baye's Theorem- Random Variables- Probability Mass Function- Probability Density Functions-Properties - Moments- Moment generating functions and their properties.

Standard Distributions: Discrete Distributions - Binomial- Poisson- Properties, Moment generating functions. Continuous Distributions - Uniform –Exponential- Normal Distributions and their properties.

Two Dimensional Random Variables: Joint distributions – Marginal and conditional distributions –Covariance – Correlation and linear regression using least square method – Transformation of random variables.

Module II **22 Hours**

Test of Hypotheses: Sampling distributions, Estimation of parameters, Statistical hypothesis, large sample test based on Normal distribution for single mean and difference of means, Tests based on t, Chi-square and F distributions for mean, variance and proportion, Contingency table (test for independent), Goodness of fit.

Design of Experiments: Analysis of Variance (ANOVA)- One Way Classification– Completely Randomized Design(CRD) – Two-way Classification – Randomized Block Design (RBD) –Latin square.

List of Experiments: **30 Hours**

1. R programming for basic arithmetic operators.
2. Probability distributions (Discrete & Continuous) using R Programming.
3. Calculate correlation coefficient using R Programming.
4. Small sample test using R Programming.
5. Large sample test using R Programming.
6. One way, two-way Classification using R Programming.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply standard distributions and the concepts of random variables, to solve real-world problems.	Apply
CO2: Use the concept of probability distributions to solve real life problems.	Apply
CO3: Using correlation coefficient and discusses the relationship between two variables.	Apply
CO4: Apply variance to analyze the samples.	Apply
CO5: Demonstrate the concepts of standard distributions and testing of hypothesis using modern tools (For Laboratory component only)	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO5	3	-	-	-	1	-	-	-	1	1	-	1	1	1

High-3; Medium-2; Low-1

Text Book(s):

T1. Veerajan T, “Probability, Statistics and Random process”, 3rd Edition, Tata McGraw-Hill, NewDelhi, 2017.

T2. Dr.J.Ravichandran, “Probability and Statistics for Engineers”, 1stEdition, Wiley India Pvt. Ltd.,2010.

Reference Book(s):

R1. R.E. Walpole, R.H. Myers, S.L. Myers, and K Ye, “Probability and Statistics for Engineers andScientists”, 9th Edition Pearson Education, Asia, 2013.

R2. M.R. Spiegel, J. Schiller and R.A. Srinivasan, “Schaum's Outlines Probability and Statistics”, 4th Edition Tata McGraw Hill edition, 2012.

R3. Morris DeGroot, Mark Schervish, “Probability and Statistics”, Pearson Educational Ltd.

Web References:

1 https://archive.nptel.ac.in/courses/111/105/111105090/

2 https://archive.nptel.ac.in/courses/111/105/111105041/

Course Code: 23EVT401		Course Title: Signals and Systems	
Course Category: Major		Course Level: Intermediate	
L:T:P(Hours/Week) 3:1:0	Credits:4	Total Contact Hours: 60	Max Marks:100

Course Objectives:

The course is intended to classify various continuous-time, discrete-time signals and systems. Also, the course imparts the spectral characteristics of continuous-time signals and systems using Fourier and Laplace transforms, and discrete time signals and systems using Z transform.

Module I **23 Hours**

CLASSIFICATION OF SIGNALS AND SYSTEMS: Continuous time signals (CT signals)-Discrete time signals (DT signals) – Step, Ramp, Pulse, Impulse, Exponential - classification of CT and DT signals – periodic and aperiodic signals, random signals, Energy & Power signals - CT and DT systems, Classification of systems.

SPECTRAL ANALYSIS OF CONTINUOUS TIME SIGNALS: Fourier series, Fourier transforms: properties – Spectral analysis of continuous time signals- Frequency response of continuous time LTI systems.

Module II **22 Hours**

SPECTRAL ANALYSIS OF DISCRETE TIME SIGNALS: Baseband Sampling of CT signals– Aliasing, Introduction to discrete Fourier series, DTFT: properties and spectral analysis of discrete time signals- Frequency response of discrete time LTI systems. **CHARACTERIZATION OF DISCRETE TIME LTI SYSTEMS:** Difference Equations-Impulse response -Convolution sum-Z-transform: properties and application in discrete time signal and system analysis.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Identify and differentiate continuous-time and discrete-time signals and systems based on their properties.	Apply
CO2: Determine the frequency domain representation and response of continuous-time signals and LTI systems using Fourier transforms.	Apply
CO3: Analyze sampling effects, including aliasing, and interpret discrete-time signal spectra using DTFT.	Analyze
CO4: Examine discrete-time LTI systems by solving difference equations and evaluating their responses and stability using Z-transform	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO4	-	3	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Allan V. Oppenheim, S. Wilsky and S.H.Nawab "Signals and System", Pearson education, 2007.

T2. Simon Haykins and Barry Van Veen, "Signals and Systems", John Wiley & Sons,2004.

Reference Book(s):

R1. HPHsu, Rakesh Ranjan,"Signals and Systems", Schaum's Outlines, Tata McGraw Hill, Indian Reprint, 2007.

R2. S. Haykin and B. Van Veen, "Signals and Systems", 2nd Edition, Wiley,2003

R3. P.Ramakrishna Rao, "Signals and Systems", Tata Mc Graw Hill Publications, 2nd Edition, 2008.

R4. Dward W. Kamen, Bonnie S. Heck, "Fundamentals of Signals and Systems, Using the Web and MATLAB", Pearson, Indian Reprint, 3rd Edition,2007

R5. John Alan Stuller, "An Introduction to Signals and Systems", Thomson,2007

Web References:

1. https://ocw.mit.edu/resources/res-6-007-signals-and-systems-spring-20112.
2. https://nptel.ac.in/courses/117/104/117104074/
3. http://www.ws.binghamton.edu/fowler/Fowler%20Personal%20Page/EECE301%20-%20Flipped.htm

Course Code: 23EVT402		Course Title: Linear Integrated Circuits	
Course Category: Major		Course Level: Intermediate	
L:T:P (Hours/Week) 3:0:0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on OPAMP internal structure, frequency characteristics and utilize the same to develop application circuits. Also, the course imparts a depth knowledge on PLL and Timer circuit design.

Module I **22 Hours**

BASICS OF OPERATIONAL AMPLIFIERS: Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations

Applications of OPAMP: Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

Module II **23 Hours**

ANALOG MULTIPLIER AND PLL: Analog Multiplier using Emitter Coupled Transistor Pair - Gilbert Multiplier cell – Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565.

WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS: Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Illustrate fundamental concepts of current mirrors, current sources, and differential amplifiers to Analyze and design the internal circuitry of operational amplifiers.	Apply
CO 2: Compare the feedback configurations to design and implement analog circuits for signal processing, filtering, and waveform generation	Analyze
CO 3: Experiment analog multiplier principles to design and implement signal processing circuits.	Apply
CO 4: Apply specialized ICs (555 Timer, PLL 565, voltage regulators) to design waveform generators, frequency control systems, and power supplies.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. J.D.Roy Choudhury,"Linear integrated Circuits",2017,5th Edition, New-Age International Publishers, Chennai.

T2. K. R. Botkar, "Integrated Circuits" 10th Edition, Kp, 2010.

Reference Book(s):

R1. Ramakant A. Gayakwad,"Op-Amps and Linear Integrated Circuits",2015,4th Edition, Pearson Education, Bangalore.

R2. Robert F.Coughlin and Frederick F.Driscoll, "Operational Amplifiers and Linear Integrated Circuits",2015, 6th Edition, Pearson Education, Bangalore.

Web References:

1. https://onlinecourses.nptel.ac.in/noc24_ee73/preview
2. https://archive.nptel.ac.in/courses/108/108/108108111/

Course Code: 23EVT403		Course Title: Microprocessors and Microcontrollers	
Course Category: Major		Course Level: Intermediate	
L:T:P (Hours/Week) 3:0:0	Credits: 3	Total Contact Hours: 45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on microprocessor and microcontroller architecture, develop programs for on-chip peripherals, and design systems using interfacing.

Module I **22 Hours**

8- BIT and 16 - BIT MICROPROCESSOR: 8085 Architecture, Interrupts, Instruction set, Timing diagrams, 8086 Architecture - Minimum and Maximum mode configurations, Instruction set, Addressing modes, Assembly Language Programming, Memory and I/O interfacing.

PERIPHERALS AND INTERFACING: Programmable Peripheral Interface (8255), Keyboard Display Controller (8279), Programmable Timer Controller (8254), Programmable Interrupt Controller (8259), Serial Communication Interface (8251), ADC0808 and DAC0808 Interface.

Module II **23 Hours**

MICROCONTROLLER: 8051 – Architecture, Special Function Registers (SFRs), I/O Ports, Timers / Counters, Interrupts, Serial communication, Instruction set, Addressing modes, Assembly language programming.

MICROCONTROLLER BASED SYSTEM DESIGN: Display Interfacing - matrix display, (16x2) LCD, Sensor and Relay, interfacing Stepper Motor, interfacing DC Motor Speed Control using PWM, RTC and EEPROM interface using I2C protocol. Sensor and Actuator interfacing with 8051 microcontrollers.

32- BIT ARM PROCESSOR: RISC Vs CISC Architecture, ARM Processor Architecture, ARM Core data flow model, Barrel Shifter, ARM processor modes and families, Pipelining, ARM instruction set and its Assembly language/Embedded C Programming.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Interpret the architecture, addressing modes and instruction set of 8085 and 8086 microprocessors to write efficient assembly language programs.	Apply
CO2: Design and implement memory and I/O interfaces for 8085/8086 microprocessors using programmable peripheral ICs.	Apply
CO3: Analyze the architectural features and functional blocks of 8051 microcontrollers to interpret their operational behaviour for specific embedded applications.	Analyze
CO4: Design and program microcontroller-based systems for interfacing sensors, actuators, and displays, utilizing 8051 and ARM processor architectures.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. R.S.Gaonkar,"Microprocessor Architecture, Programming and Applications with the 8085", 5th Edition, Prentice Hall, 2002.

T2. Muhammad ALI Mazidi, RolinD.Mckinlay, Danny Causery,"PIC Microcontroller and Embedded systems using assembly and C PIC18", Pearson international edition, 2008.

Reference Book(s):

R1. A.K Ray , K.M.Bhurchandi ,"Advanced Microprocessors and Peripherals" 3rd Edition McGraw Hill Education 2012

R2. Steve Furber, "ARM System-on-Chip Architecture" Pearson Education Limited, 2012

R3. Krishna Kant, "Microprocessor and Microcontroller Architecture, Programming and System Design using 8085, 8086, 8051 and 8096", PHI, 2011.

Web References:

1. https://www.nxp.com/docs/en/user-guide/UM10139.pdf
2. http://www.microchip.com/design-centers/microcontrollers
3. https://electrosome.com/category/tutorials/pic-microcontroller/hi-tech-c/
4. https://ww1.microchip.com/downloads/en/devicedoc/39582b.pdf

Course Code: 23EVI404		Course Title: Fundamentals of VLSI	
Course Category: Major		Course Level: Intermediate	
L:T:P(Hours/Week) 3:0:0	Credits:3	Total Contact Hours: 75	Max Marks:100

Course Objectives:

To introduce students to CMOS device and circuit design, focusing on delay, power, and interconnect analysis through simulation and characterization.

Module I **22 Hours**

Introduction to VLSI: History & evolution of CMOS VLSI, Design abstraction levels (behavioural → physical), Overview of a simple MIPS microprocessor. **MOS Transistor Theory:** Long‑channel I‑V characteristics, Gate & diffusion capacitances (C–V), Non-ideal effects: velocity saturation, channel‑length modulation, leakage, Static inverter DC curves & noise margins

CMOS Processing Technology: Wafer formation, photolithography, well/channel formation Oxide growth, gate/source/drain formation, metallization, passivation, Design rule checking, layout design rules, stick diagrams, Process enhancements & DRC/EXTRACT flows.

Module II **23 Hours**

Delay Modeling: Propagation and contamination delay, RC Delay Estimation, and model basics. **Logical Effort Method:** Gate and path sizing principles, key limitations. **Power Dissipation:** Dynamic and static power overview, Activity factor, voltage, frequency, and capacitance trade-offs, Basics of leakage reduction and power gating. **Interconnects: Wire Modeling:** Resistance and capacitance in interconnects, Delay, energy, and crosstalk considerations.

Combinational Circuits: Static CMOS Logic: NAND, NOR, AOI, and complex gates, **Alternative Logic Styles:** Pseudo-NMOS, pass-transistor, and transmission gate logic **Dynamic Logic Basics:** Domino logic and charge sharing issues **Sequential Circuits:** Latches and Flip-Flops: Master-slave and pulsed flip-flops, Timing Constraints: Setup, hold, and clock skew, **Clocking Methodologies:** Static sequencing overview.

List of Experiments: **30 Hours**

1. R programming for basic arithmetic operators.
2. Probability distributions (Discrete & Continuous) using R Programming.
3. Calculate correlation coefficient using R Programming.
4. Small sample test using R Programming.
5. Large sample test using R Programming.
6. One way, two-way Classification using R Programming.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Illustrate the principles of MOS transistor theory and CMOS inverter characteristics to analyze DC behavior and noise margins.	Apply
CO 2: Explain CMOS fabrication steps and design rules to interpret layout constraints and technology-aware circuit design flow.	Apply
CO 3: Articulate delay modeling and logical effort techniques to size gates and analyze performance trade-offs in CMOS circuits.	Apply
CO 4: Analyze power dissipation mechanisms and interconnect effects to evaluate energy and timing in combinational and sequential circuits.	Analyze
CO5: Experiment and characterize CMOS circuits and devices with parametric and performance analyses.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO5	3		-	-	1	-	-	-	1	1	2	1	1	1

High-3; Medium-2; Low-1

Text Book(s):

T1.Weste, Neil H. E., and David Harris. CMOS VLSI Design: A Circuits and Systems Perspective. 4th ed., Pearson Education, 2010.

Reference Book(s):

R1.M.Morris Mano and Michel.D.Ciletti, “Digital Design with an introduction to HDL,VHDL and Verilog”, 6th edition Pearson education.

Web References:

1. https://nptel.ac.in/courses/117106092

Course Code: 23EVL401		Course Title: Linear Integrated Circuits Laboratory	
Course Category: Major		Course Level: Intermediate	
L: T:P (Hours/Week) 0:0 :4	Credits:2	Total Contact Hours:60	Max Marks:100

Course Objectives:

The course is intended to incorporate knowledge on design and analysis of simple linear integrated circuits using OP-AMP ICs.

List of Experiments: **60 Hours**

1. Design of Inverting, Non-Inverting amplifiers, and Voltage follower.
2. Perform mathematical operations using operational amplifier.
3. Design of Instrumentation amplifier.
4. Design and testing of Precision Rectifier.
5. Design of Comparator and Schmitt trigger circuits.
6. Design of Square wave generator for a specified frequency and duty cycle, using operational amplifier IC741.
7. Design of Triangular wave generator.
8. Design of a Sinusoidal oscillator for specified frequency – Wien-bridge and RC phase shift oscillators using IC741.
9. Design and testing of Active filters - LPF and HPF for specified frequency.
10. Design of Astable and Monostable Multivibrators using IC555.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Examine simple analog circuits to perform mathematical operations, rectification, and analog comparison.	Apply
CO 2: Examine waveform generators, multivibrators, A/D and D/A converters.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	1	-	-	-	1	1	-	1	1	1
CO2	3	-	-	-	1	-	-	-	1	1	-	1	1	1

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code: 23EVL402		Course Title: Microprocessors and Microcontrollers Laboratory	
Course Category: Major		Course Level: Intermediate	
L: T:P (Hours/Week) 0:0 :3	Credits: 1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on developing programs to perform arithmetic operations with 8085 Microprocessor, application development with interfacing techniques in PIC16Fxx/LPC2148.

List of Experiments: **45 Hours**

1. Programs for 8 /16-bit Arithmetic, Sorting and Searching operations in 8085 and 8086.
2. 7 segment display with 8085 or 8086 using 8255 interfaces.
3. Stepper and DC motor control using 8085 or 8086 microprocessors.
4. Interfacing ADC, DAC with 8085 or 8086 microprocessors.
5. Configuring and programming Timer and Interrupts in 8051 microcontrollers.
6. Data transmission and reception using UART in 8051 microcontrollers.
7. Interfacing LED, LCD, Switch and 4x4 Keypad with ARM processor.
8. Interfacing Sensor and Actuator with ARM processor.
9. Configuring and Programming of Timers/Counters and Interrupts in ARM Processor.
10. UART and SPI Interfacing using ARM processor.
11. Interfacing RTC and EEPROM with 8051 or ARM processor.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Analyze the timing and control sequences required to interface various peripheral devices (e.g., 7-segment displays, motors, ADCs/DACs) with 8085/8086 microprocessors, evaluating the efficiency of chosen interfacing techniques.	Analyze
CO2: Analyze the role of timers, interrupts, and communication protocols (UART, SPI, I2C) in managing real-time data flow and concurrent operations within 8051 and ARM processor-based embedded systems.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	1	1	-	1	1	1
CO2	-	3	-	-	-	-	-	-	1	1	-	1	1	1

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code: 23ESL401		Course Title : Professional Skills 3- Professional Development and Etiquette (Common to all B.E/B.Tech Programmes)	
Course Category: SEC		Course Level: Intermediate	
L: T:P (Hours/Week) 0: 0: 2	Credits: 1	Total Contact Hours:30	Max Marks:100

Course Objectives:

The course is intended to cultivate students' appropriate etiquette across various personal and professional contexts, fostering professionalism and effective communication.

Module I **15 Hours**

Emotional Intelligence

Intrapersonal Skill: Goal Setting- Self-management- Emotional Intelligence: Understanding & Developing EI for Effective Communication and Relationships –Enhancing Social Skills

Professional Development

Introduction to Professional Development - Career State Assessment - Set Career Goals- Stay on Industry Trends - Self & Lifelong learning – Creativity - Problem Solving Skills - Strong Fundamentals – Using/ Creating Opportunities – Work & Life Balancing - Revisiting Goals

Teamness and Interpersonal skills

Paraphrasing: Techniques for Active Listening -Paraphrasing as a Tool for Effective Understanding and Communication – Collaboration and Team Building: Building Trust and Rapport - Self-paced learning.

Module II **10 Hours**

Effective Communication

Effective Verbal Communication - Assertive Communication - Elements of Effective Communication - Barriers to Effective Communication - Persuasion Skills - Effective Presentation: Oral and visual presentation – Drafting formal reports.

Professional Etiquette

Introduction - Types of professional Etiquette- Personal Grooming: Importance of Personal Grooming in Professional Settings- Dress Codes and Professional Appearance Guidelines- Body language - Social – Email – Telephonic – Dining – Classroom -

Activities:

- Emotional Intelligence: Scenario based role play, Debate
- Paraphrasing: Listening, Reading
- Effective Presentation:
  - Oral Presentation: Self-Introduction, JAM, Extempore speech
  - Visual presentation: Email Writing, Power Point Presentation, Vlog
- Professional Etiquette: Demonstrate required
- Professional Etiquette in all the above activities.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Communicate effectively and exhibit Professional etiquettes in various social forums.	**Apply**

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	2	2	3	-	1	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1: Sabina Pillai, Agna Fernandez, “Soft Skills & Employability Skills”, Cambridge University Press2018

T2: Peggy Post &Peter Post, “The Etiquette Advantage in Business: Personal Skills for Professional Success”, 2nd edition (May 3, 2005), William Morrow.

Reference Book(s):

R1: Ashraf Rizvi, "Effective Technical Communication" 2nd Edition, McGraw-Hill India, 2018

R2: Maithry Shinde, Jyotsna Sreenath, “Life Skills & Personality Development”, Cambridge University Press 2022

Web References:

1. https://www.indeed.com/career-advice/career-development/etiquette-at-work
2 https://www.skillsyouneed.com/interpersonal-skills.html

Passed in 4th Board of Studies Meeting held on 16.12.2024
Approved in 19th Academic Council Meeting held on 03.01.2025 BoS Chairman

SEMESTER V

Course code: 23EVT501		Course Title: Control Systems	
Course Category: Major		Course level : Higher	
L:T:P(Hours/Week) 3: 1: 0	Credits:4	Total Contact Hours:60	Max Marks:100

Course Objectives:

The course introduces the fundamentals of control systems covering system components, modeling techniques, time response, frequency response, stability analysis, compensator design, PID controllers, state-space representation, digital control methods, controllability, and observability concepts.

Module I **22+8 Hours**

Components of the Control System: Terminology and Basic Structure-Feed forward and Feedback control theory Electrical and Mechanical Transfer Function Models-Block Diagram Models-Signal flow graphs models-DC and AC servo Systems-Synchronous - Multivariable control system.

Time Response with System Design: Transient response-steady state response - Measures of performance of the standard first order and second order system-effect on an additional zero and an additional pole-steady error constant and system- type number-PID control -Analytical design for PD, PI, PID control systems

Module II **23+7 Hours**

Frequency Response with System Analysis: Closed loop frequency Response-Performance specification in frequency domain Frequency response of standard second order system- Bode Plot - Polar Plot- Nyquist plots -Design of compensators using Bode plots- Cascade lead compensation Cascade lag compensation -Cascade lag-lead compensation.

Stability Analysis: Concept of stability -Bounded - Input Bounded - Output stability -Routh stability criterion -Relative stability -Root locus concept -Guidelines for sketching root locus Nyquist stability criterion.

Control System Analysis: State variable representation -Conversion of state variable models to transfer functions -Conversion of transfer functions to state variable models - Solution of state equation -Concepts of Controllability and Observability-Stability of linear systems Equivalence between transfer function and state variable representations -State variable analysis of digital control system -Digital control design using state feedback.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the basic concepts of control system to model systems and simplify representations using transfer functions, block diagrams, and signal flow graphs.	Apply
CO 2: Analyze the time-domain response, stability, and error characteristics of control systems using test inputs, root locus, and Routh-Hurwitz criteria.	Analyze
CO 3: Apply frequency response to determine performance specifications, construct plots, and analyze system stability.	Apply
CO 4: Analyze dynamic systems using state space representations, evaluate stability through eigenvalues and state transition matrices, and assess controllability and observability.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	-	3	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. J. Nagrath and M.Gopal, “Control System Engineering”, New Age Internationa Publishers, 7th Edition, 2021.

T2. K. Ogata, “Modern Control Engineering”, PHI, 5th Edition, 2012.

Reference Book(s):

R1. S.K. Bhattacharya, “Control System Engineering”, Pearson, 3rd Edition, 2013.

R2. Benjamin.C. Kuo, “Automatic Control Systems”, Prentice Hall of India, 10th Edition,2017.

Web References:

1. https://archive.nptel.ac.in/courses/107/106/107106081/

Course Code: 23EVT502		Course Title: HDL Programming	
Course Category: Major		Level: Higher	
L:T:P(Hours/Week) 3 : 0: 0	Credits: 3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The Course intends to provide a foundational understanding of HDLs, focusing on modeling, simulation, and synthesis of digital logic using VHDL and Verilog, with hands-on experience in FPGA implementation and verification using industry-standard tools.

Module I **22 Hours**

Introduction to HDL and VHDL: Need for hardware description languages, abstraction levels, design flow, overview of VHDL vs Verilog. **VHDL Language Elements:** Entity and architecture, data types, operators, signals vs variables, concurrent and sequential statements. **Modeling Styles in VHDL:** Behavioural, dataflow, and structural modeling

Design Examples Using VHDL: Combinational circuits – adders, multiplexers, encoders, decoders. **Sequential Circuits in VHDL:** Flip-flops, counters, shift registers, finite state machines. **Testbenches and Simulation:** Writing simple testbenches, waveform analysis, simulation practices using tools (ModelSim/Xilinx Vivado). **Synthesis Guidelines:** Synthesizable vs non-synthesizable constructs, constraints for synthesis

Module II **23 Hours**

Introduction to Verilog: Basic constructs, modules, ports, nets, registers, operators, Design Methodology in Verilog: Hierarchical design, parameterized modules. **Combinational Logic in Verilog:** Continuous assignment, case statements, if-else constructs. **Sequential Logic in Verilog:** Always blocks, edge-triggered behavior, blocking vs non-blocking assignments. **Advanced Verilog Constructs:** Generate Statements, System Tasks and Functions, Assertion. **FSM Design Using Verilog:** Mealy and Moore machines, practical examples. **Testbenches in Verilog:** Stimulus generation, waveform analysis, debugging **Synthesis and FPGA Mapping:** Using synthesis tools (Vivado/Quartus), RTL view, resource estimation.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply VHDL modeling styles to design and simulate combinational and sequential digital circuits.	Apply
CO 2: Analyze the functionality and synthesis results of VHDL-based digital systems using simulation tools.	Analyze
CO 3: Use Verilog to describe, model, and implement hierarchical digital systems with proper timing behavior.	Apply
CO 4: Analyze and interpret simulation outputs and synthesis reports to verify and optimize Verilog designs for FPGA targets.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	2
CO2	-	3	-	-	-	-	-	-	-	-	-	-	1	2
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	2
CO4	-	3	-	-	-	-	-	-	-	-	-	-	1	2

High-3; Medium-2;Low-1

Text Book(s):

T1. "Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog" by M. Morris Mano and Michael D. Ciletti, 6th Edition, Pearson, 2017.

Reference Book(s):

R1. "The Designer's Guide to VHDL" by Peter J. Ashenden, 3rd Edition, Morgan Kaufmann Publishers, 2008.

R2. "A VHDL Primer" by J. Bhasker, 3rd Edition, Prentice Hall, 1999.

R3. "Verilog HDL: A Guide to Digital Design and Synthesis" by Samir Palnitkar, 2nd Edition, Pearson Education, 2003.

R4. "HDL Programming (VHDL and Verilog)" by Nazeih M. Botros, Charles River Media, 2006

Web References:

1 https://nptel.ac.in/courses/117105080
2 https://nptel.ac.in/courses/117106086

Course code: 23EVT503		Course Title: Analog IC Design	
Course Category: Major		Course level: Higher	
L:T:P(Hours/Week) 3: 0: 0	Credits: 3	Total Contact Hours: 45	Max Marks:100

Course Objectives:

The course is to explore the design and analysis of analog CMOS circuits, focusing on device modeling, multi-transistor stages, frequency response, noise analysis, operational amplifiers, and feedback stability techniques.

Module I **22 Hours**

Basic Building Blocks: NMOS and PMOS device operation in saturation and sub-threshold regions, device transconductance, output impedance and equivalent circuit. Introduction to Device models for simulation. CG, CG, and source follower circuits. gm/Id design methodology.

Multiple Transistor Stages: Cascode circuits. folded cascode circuits, Differential amplifier circuits, quantitative analysis of differential pair, CMRR, Differential pair with MOS loads, Gilbert Cell, Current Mirrors.

Frequency Response, Noise: Frequency response of CS and CG stages. Miller effect and association of poles with nodes. Characteristics of noise – thermal and flicker noise. Noise in

Module II **23 Hours**

Operational Amplifiers: Two stage op-amps, gain boosting, common mode feedback, input range limitation, slew rate, power supply rejection, noise in op-amps**.**

Feedback and Stability: Properties of feedback circuits, topologies, effect of loading and noise in feedback circuits. Stability in multipole systems, phase margin, frequency compensation in two stage op-amps, other compensation techniques.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Identify the operating regions of MOS transistors and the structure of basic analog building blocks such as CS, CG, and source follower circuits.	Apply
CO 2: Construct multi-transistor analog circuits including differential pairs, cascode stages, and current mirrors with frequency response considerations.	Apply
CO 3: Develop two-stage operational amplifiers with performance parameters such as gain, slew rate, PSRR, and input range.	Apply
CO 4: Design stable feedback systems using compensation techniques for multipole analog circuits.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	3

High-3; Medium-2;Low-1

Text Book(s):

T1. B. Razavi, “Design of CMOS Analog Integrated Circuits", Tata McGraw Hill, 2002.

T2. Paul R. Allen and Douglas R. Holberg**,** *CMOS Analog Circuit Design*, Oxford University Press, 3rd Edition, 2012.

Reference Book(s):

R1. D.A. Johns and K. Martin, Analog Integrated Circuit Design*, Wiley, 2012*

R2. Thomas H. Lee*,* The Design of CMOS Radio-Frequency Integrated Circuits*,* Cambridge University Press, 2nd Edition, 2004.

Web References:

1 nptel.ac.in/courses/117106030

Course Code: 23EVL501		Course Title: HDL Programming Laboratory	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 0: 0: 3	Credits: 1.5	Total Contact Hours: 45	Max Marks:100

Course Objectives:

The course enables students to gain practical knowledge in digital system design using hardware description languages, focusing on modeling, simulation, synthesis, and verification of combinational and sequential circuits using VHDL and Verilog, with a strong emphasis on Verilog for real-world digital design applications.

List of Experiments: **45 Hours**

1. HDL Implementation and Verification of Basic Logic Gates.
2. Modeling and Simulation of Half and Full Adders using HDL.
3. Modeling, Simulation and Testbench for Half and Full Subtractors.
4. Design and Simulation of 4-bit Ripple Carry Adder.
5. Design and Simulation of 4:1 Multiplexer and 1:4 Demultiplexer using HDL.
6. Design, Simulation and Testbench of 8-to-3 Encoder and 3-to-8 Decoder.
7. Design and Simulation of D and JK Flip-Flops with Timing Analysis using HDL.
8. Design and Simulation of 4-bit SISO, SIPO, PISO, and PIPO Shift Registers using HDL.
9. Modeling and Simulation of 4-bit Synchronous and Asynchronous Counters.
10. Design and Simulation of 4-bit Comparator using HDL.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply VHDL to model and simulate basic combinational and sequential logic circuits.	Apply
CO2: Develop Verilog-based designs for arithmetic, data routing, and control circuits using behavioral and structural modeling.	Apply
CO3: Analyze the functionality and timing behavior of digital systems through simulation and waveform interpretation	Analyze
CO4: Design and verify digital systems like FSMs using Verilog, suitable for implementation on programmable hardware platforms.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	1	-	-	-	1	1	-	1	3	3
CO2	3	-	-	-	1	-	-	-	1	1	-	1	3	3
CO3	-	3	-	-	1	-	-	-	1	1	-	1	3	3
CO4	3	-	-	-	1	-	-	-	1	1	-	1	3	3

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course code: 23EVL502		Course Title: Analog IC Laboratory	
Course Category: Major		Course level: Higher	
L:T:P(Hours/Week) 0: 0: 3	Credits:1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to design, simulate, and analyze fundamental CMOS analog circuits using industry-standard tools, developing practical insight into amplifier stages, current mirrors operational amplifiers, and layout methodologies.

List of Experiments: **45 Hours**

1. Common Source Amplifier - Design, Simulation, and Performance Analysis.
2. Layout Implementation of Common Source Amplifier with DRC & LVS Checks.
3. Common Drain Amplifier - Design, Simulation, and Performance Analysis.
4. Layout Design and Verification of Common Drain Amplifier: DRC and LVS Checks.
5. Common Gate Amplifier - Design, Simulation, and Performance Analysis.
6. Layout Design of Common Gate Amplifier with DRC and LVS Verification.
7. Design, Simulation, and Analysis of Current Mirror Circuit using CMOS technology.
8. Layout Design and Verification of Current Mirror Circuit using DRC and LVS Checks.
9. Design and Performance Evaluation of a Differential Amplifier.
10. Two-Stage Op-Amp Design with DC, AC, and Transient Analysis.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Design and simulate fundamental CMOS building blocks such as amplifiers and current mirrors using EDA tools.	Apply
CO2: Analyze the performance of differential amplifier stages and characterize gain, CMRR, and output swing.	Analyze
CO3: Implement and evaluate CMOS operational amplifiers including single-stage and two-stage designs with compensation.	Apply
CO4: Perform layout, parasitic extraction, and system-level integration of analog circuits and assess their performance post-layout.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	3	-	1	-	-	-	1	1	-	1	3	3
CO2	-	3	-	-	1	-	-	-	1	1	-	1	3	3
CO3	3	-	-	-	1	-	-	-	1	1	-	1	3	3
CO4	-	3	-	-	1	-	-	-	1	1	-	1	3	3

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code: 23EVP501		Course Title: Reverse Engineering Project	
Course Category: Project		Course Level: Higher	
L:T:P(Hours/Week) 0:0:6	Credits: 3	Total Contact Hours: 90	Max Marks:100

Course Objectives:

The course encourages students to investigate how existing technologies work by systematically breaking down systems, interpreting their operation, and reconstructing their behaviour through analytical and creative approaches

Module I **45 Hours**

Overview of reverse engineering practices – Ethical considerations and real-world examples – Selection and approval of a project system – Structural breakdown and functional interpretation.

Module II **45 Hours**

Mapping operational flow and system behavior – Creating conceptual or simulated models – Evaluating performance characteristics – Proposing enhancements or alternative implementations.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Analyze and interpret the internal structure and working principles of existing systems through systematic investigation	Analyze
CO2: Apply logical reasoning and critical thinking to abstract functional behavior from complex designs or products	Apply
CO3: Develop models or simulations that reflect the functionality and architecture of the analyzed system.	Evaluate
CO4: Demonstrate problem-solving and innovation skills by suggesting improvements or alternative design approaches.	Create

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	-	-	-	3	1	-	-	-	-	-	-	-	3	3
CO4	-	-	3	-	-	-	-	-	2	2	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. K. T. Ulrich and S. D. Eppinger*,* Product Design and Development*, 6th* ed., New York, NY, USA: McGraw-Hill, 2016.

T2. Eldad Eilam, “Reversing: Secrets of Reverse Engineering”. Indianapolis, IN, USA: Wiley Publishing, April 2005.

Web References:

1. J. Platt, “An industrial approach to reverse engineering,” in Proc. IEEE Int. Conf. on Engineering Education, Vancouver, BC, Canada, July 2005, pp. 6–10.

SEMESTER VI

Course code: 23EVT601		Course Title: Digital IC Design	
Course Category: Major		Course level: Higher	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course aims to equip students with skills in designing and analysing digital integrated circuits using CMOS technology. It emphasizes efficient circuit implementation through combinational, sequential, and dynamic logic design, focusing on speed, power, and reliability.

Module I **22 Hours**

Introduction to Digital IC Design: Evolution of digital ICs, CMOS technology trends and scaling challenges, **MOS Transistor Theory and CMOS Inverter:** MOSFET, structure and operation, **I–V characteristics and regions of operation, Second-Order Effects,** CMOS inverter static and dynamic behaviour, Noise margins, delay, and power estimation

Combinational Logic Gates: Static CMOS logic: NAND, NOR, and compound gates, Logic effort and delay modeling, Design trade-offs: area, delay, power. **Alternative Logic Styles:** Pass-transistor logic, Transmission gate logic, Comparison of static vs. dynamic logic, **Interconnect and Scaling Effects:** Resistance, capacitance, and delay in interconnects, Buffering techniques and repeater insertion, Scaling effects and impact on performance. **Design Considerations and Trade-offs:** Sizing for performance, Delay–power trade-offs, Technology-aware design decisions

Module II **23 Hours**

Sequential Circuit Design: Latches and flip-flops (static and dynamic), Setup/hold time, timing constraints, Pipelining and register design. **Clocking and Timing Strategies:** Clock distribution, skew, and jitter, Synchronous vs. asynchronous design. **Power Dissipation and Optimization:** Sources of power consumption, Dynamic, short-circuit, and leakage power, Low-power design techniques (voltage scaling, clock gating).

Memory Design Fundamentals: SRAM and DRAM cell design, Peripheral circuits: decoders, sense amplifiers, Memory timing and optimization. **Design Flow and Methodologies:** Custom vs. semi-custom design, Standard cell libraries, floor planning, Intro to layout, DRC, LVS.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the principles of MOSFET operation and CMOS inverter characteristics to Analyze and estimate performance parameters such as noise margins, delay, and power in basic digital circuits.	Apply
CO 2: Analyze the performance, area, and power trade-offs of various CMOS logic styles and interconnect strategies to evaluate their impact on delay and scalability in digital circuit design.	Analyze
CO 3: Analyze the behaviour of sequential elements and clocking strategies to identify timing constraints and evaluate power optimization techniques in digital circuit design.	Analyze
CO4: Demonstrate the design of basic memory cells and apply standard digital design methodologies, including layout and verification techniques, for memory and logic circuit implementation.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO4	-	-	3	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. "Digital Integrated Circuits: A Design Perspective" by Jan M. Rabaey, 2nd Edition, 2003

Reference Book(s):

R1 “CMOS Digital Integrated Circuits, Analysis and Design” Revised 4th Edition by Sung-Mo Kang and Yusuf Leblebici, 2019.

R2 "Digital VLSI Chip Design with Cadence and Synopsys CAD Tools" by Erik Brunvand, 1st Edition, 2009.

R3 " CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Harris, 4th Edition, 2010.

Web References:

1. https://nptel.ac.in/courses/117/105/117105082/
2. https://www.cse.iitb.ac.in/~mythili/courses/cs731/

Course Code: 23EVT602		Course Title: VLSI Digital Signal Processing	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3: 0: 0	Credits: 3	Total Contact Hours: 45	Max Marks:100

Course Objectives:

The course is intended to apply advanced architectural techniques such as pipelining, parallel processing, retiming, unfolding, strength reduction, and wave pipelining to optimize digital signal processing systems, with a focus on efficient filter design, fast convolution, bit-level arithmetic architectures, and numerical optimization strategies.

Module I **22 Hours**

PIPELINING AND PARALLEL PROCESSING: Introduction to DSP Systems, Typical DSP algorithms, Data flow graph representations, Loop bound and Iteration bound, Longest Path Matrix algorithm; Pipelining and Parallel processing of FIR digital filters, Pipelining and Parallel processing for low power.

RETIMING AND ALGORITHMIC STRENGTH REDUCTION: Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, Odd-Even Merge-Sort architecture, Parallel Rank Order filters.

FAST CONVOLUTION AND COMBINED PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS: Fast convolution – Cook-Toom algorithm, Modified Cook-Took algorithm; Look- Ahead pipelining in first- order IIR filters, Look- Ahead pipelining with power-of-two decomposition, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters

Module II **23 Hours**

BIT-LEVEL ARITHMETIC ARCHITECTURES: Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, 4x 4 bit Baugh Wooley carry-save multiplication tabular form and implementation, CSD representation, CSD multiplication using Horner‘s rule for precision improvement, Distributed Arithmetic.

NUMERICAL STRENGTH REDUCTION AND WAVE PIPELINING: Numerical Strength Reduction – subexpression elimination, Multiple Constant Multiplications, Synchronous pipelining and Clocking styles, Clock skew in edge-triggered single-phase clocking, Wave pipelining.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply pipelining, parallel processing, retiming, and algorithmic strength reduction techniques to optimize DSP systems and filter architectures for performance and low power.	Apply
CO 2: Apply fast convolution and advanced pipelining-parallel processing techniques to enhance the performance of IIR filter architectures	Apply
CO 3: Apply bit-level arithmetic techniques to design and implement efficient multipliers and distributed arithmetic architectures.	Apply
CO4: Apply numerical strength reduction and wave pipelining techniques to optimize arithmetic operations and improve timing performance in digital systems.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Keshab K. Parhi, “VLSI Digital Signal Processing Systems”, Design and implementation Wiley, Inter Science, Reprint 2008.

Reference Book(s):

R1. Roger Woods, John MCAllister, Gaye Light body and Ying Yi, “FPGA based implementation of Signal Processing systems”, Wiley 2nd edition, 2011.

R2. Shoab Ahmed Khan, “Digital design of signal processing systems- A Practical Approach”, A John Wiley and Sons, Ltd., publication, 2011.

R3. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing” , McGraw-Hill, 1994

Web References:

1 https://onlinecourses.nptel.ac.in/noc20_ee44/preview

Course Code: 23EVT603		Course Title: FPGA based System Design	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3: 0: 0	Credits: 3	Total Contact Hours: 45	Max Marks:100

Course Objectives:

Course enables the design and development of digital systems using FPGA technologies by covering FPGA architectures, VLSI fundamentals, programmable fabrics, placement and routing strategies, and implementation of embedded and DSP applications with emphasis on vendor-specific tools like Xilinx.

Module I **22 Hours**

FPGA Based Systems: Introduction Basic Concepts - Digital Design and FPGA's - FPGA Based System Design - VLSI Technology Behind FPGA/CPLD - Manufacturing Processes - CMOS Logic Gates Wires - Registers and RAM -Packages and Pads.

FPGA FABRICS: FPGA Fabrics-SRAM Based FPGAs - Permanently Programmed FPGAs – Chip I/O-Circuit Design of FPGA Fabrics - Architecture of FPGA Fabrics.

Module II **23 Hours**

Overview of FPGA Architectures and Technologies: FPGA Architectural options, coarse vs fine grained, vendor specific issues (emphasis on Xilinx FPGA), Antifuse, SRAM and EPROM based FPGAs, FPGA logic cells, interconnection network and I/O Pad.

Placement and Routing: Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications -Embedded system design using FPGAs, DSP using FPGAs.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply fundamental concepts of digital design and VLSI technology to develop FPGA-based systems.	Apply
CO 2: Apply knowledge of FPGA fabric architectures to design and implement digital circuits using various FPGA technologies.	Apply
CO 3: Apply architectural features of FPGAs to design digital systems using vendor-specific technologies like Xilinx.	Apply
CO4: Apply placement, routing, and partitioning techniques to implement embedded and DSP applications on FPGAs.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Wayne Wolf, FPGA-Based System Design Verlag: Prentice Hall, 2004

T2. Wayne Wolf, Modern VLSI Design: System-on-Chip Design (3rd Edition) Verlag, 2002

Reference Book(s):

R1. S. Trimberger, Edr Field Programmable Gate Array Technology, 1994, Kluwer Academic

R2. P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, 1994, Prentice Hall

R3. S. Brown, R.J. Francis, J. Rose, Z.G. Vranesic, Field programmable gate array, 2007, Springer New York, NY

Web References:

1. https://nptel.ac.in/courses/117108040

Course Code: 23EVL601		Course Title: Digital IC Design Laboratory	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 0: 0: 3	Credits:1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

To impart practical knowledge and hands-on experience in RTL design, functional verification, synthesis, and physical design of digital circuits using industry-standard EDA tools. The course emphasizes the impact of PVT variations, critical timing paths, and design closure techniques.

List of Experiments: **45 Hours**

1. Design and simulate with test bench a full adder using 3 modeling styles.
2. Design and simulate sequence detector (finite state machine).
3. Design, simulate and synthesis reports for an ALU which perform ADD, SUB, AND, OR,1's & 2's compliment, Multiplication and Division.
4. Write Verilog code with test bench, synthesize the design and analyze the reports and critical path for 4 bit up/down asynchronous counter.
5. Analyze the changes in delay for inverter at different PVT corners.
6. Evaluate the impact of process variation on a simple digital circuit like a ripple carry adder.
7. Characterize a D flip-flop for setup and hold time across corners.
8. Perform floor planning, power planning, placement, CTS, routing and post layout simulation for ALU.
9. Perform physical design and post layout simulation for a ripple carry adder.
10. Perform physical design and sign-off verification process for a 8-to-3 priority encoder.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Design and verify digital systems using Verilog HDL, covering RTL to gate-level implementations with functional and timing simulations.	Apply
CO2: Apply industry-standard EDA tools to perform complete physical design flow and sign-off verification for complex digital circuits.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	1	-	-	-	1	1	-	1	1	1
CO2	3	-	-	-	1	-	-	-	1	1	-	1	1	1

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code: 23EVL602		Course Title: FPGA Based System Design Laboratory	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 0: 0: 3	Credits:1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on design of combinational, sequential circuits, logic controllers for real time systems, and implement the same on FPGA.

List of Experiments: **45 Hours**

1. Design and Implementation of Synchronous and Asynchronous Counters
2. Design and Implementation of a 4 bit ALU using FPGA
3. Develop a Verilog module for 4-bit Array Multiplication and 4-bit Booth Multiplication and Synthesize the designs and implement them on an FPGA device for hardware validation.
4. Develop a Verilog module for 4-bit Booth Multiplication and Synthesize the designs and implement them on an FPGA device for hardware validation.
5. Develop a Verilog module to implement a clock divider circuit that generates output clocks with frequencies equal to 1/2, 1/3, and 1/4 of the given input clock
6. FPGA-based LCD Controller / 7-Segment Display Interface
7. PWM Signal Generation using FPGA
8. Design Traffic Light Controller and perform FPGA implementation.
9. Design Vending Machine Controller and perform FPGA implementation.
10. Design FSM based Sequence Detector and perform FPGA implementation.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Design combinational and sequential digital circuits using HDL and simulate them.	Apply
CO2: Develop finite state machines and digital controllers for real-time applications.	Apply
CO3 : Interface external peripherals with FPGA and analyze signal behavior using debugging tools.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	1	-	-	-	1	1	-	1	3	3
CO2	3	-	-	-	1	-	-	-	1	1	-	1	3	3
CO3	3	-	-	-	1	-	-	-	1	1	-	1	3	3

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code:23ESL601	Course Title: Professional Skills 5: Ace and Elevate : Aptitude and Soft Skills (Common to all B.E/B.Tech Programmes)		
Course Category: SEC		Course Level: Higher	
L:T:P (Hours/Week) 0: 0: 2	Credits: 1	Total Contact Hours: 30	Max Marks: 100

Course Objectives:

To enhance students' problem-solving skills in the aptitude segment while also equipping them with effective communication skills for professional settings and success in the interview process.

Module I **15 Hours**

Verbal Ability

Parts of Speech – Tenses – Subject Verb Agreement – Synonyms – Antonyms – Idioms and Phrases - One Word Substitution – Reading Comprehension – Cloze test – Error Spotting.

Verbal Enhancement

Self-Introduction – Just A Minute- Picture Perception - Writing Skills: Sentence Types (Simple, Compound, Complex), Email drafting.

Campus to Corporate

Professional Grooming –Group Discussion – Impromptu – Interview.

Module II **15 Hours**

Quantitative Ability

Simplification & Approximation, Number System, Percentage, Averages, Ratios and Proportion, Ages, Profit & Loss, Interest Calculation, Time and work, Time, speed and distance, Clocks and Calendar, Mixtures and alligation, Permutations and Combinations, Probability, Mensuration, Data Interpretation, Data Sufficiency

Reasoning Ability

Seating Arrangement, Blood relations, Directions Problems, Syllogisms, Number & Alpha Series, Coding and Decoding, Non Verbal Reasoning, Analogies, Cubes and Dices.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Exhibit strong problem-solving skills in the aptitude segment while enhancing their communication abilities for professional settings, enabling them to excel in interviews and placement processes.	**Apply**

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	-	-	-	-	-	-	2	3	3	-	1	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Technical Communication, 3E: Principles and Practice book. Authors. Meenakshi Raman, Sangeeta Sharma, 2006

T2. Pease, Allan, and Barbara Pease. "The Definitive Book of Body Language." Bantam, 2006.

T3. Dr. R. S. Aggarwal. “Quantitative Aptitude for Competitive Examinations” Sultan Chand & Sons Pvt. Ltd, New Delhi, 2024

T4. Dr. R. S. Aggarwal. “A Modern Approach to Verbal and Non-Verbal”, Sultan Chand & Sons Pvt. Ltd, New Delhi, 2024

Reference Book(s):

R1. Cheryl Hamilton, “Communicating for Results: A Guide for Business and the Professions.”

R2. Whitcomb, Susan Britton. Resume Magic: Trade Secrets of a Professional Resume Writer. JIST Works, 2010.

R3. Carnegie, D. (2009). The Quick and Easy Way to Effective Speaking. Pocket Books.

R4. Arun Sharma. “Quantitative Aptitude for Common Aptitude Test”, McGraw Hill Publications, 5th Edition, 2020

R5. Arun Sharma. “Logical Reasoning for Common Aptitude Test”, McGraw Hill Publications, 6th Edition, 2021.

Web References:

1. https://www.linkedin.com/pulse/interview-etiquette-dos-donts-interviews-brian-vander-waal-fmy8e/
2. https://www.simplilearn.com/group-discussion-tips-article
3. https://talentbattle.in
4. https://www.geeksforgeeks.org/aptitude-questions-and-answers/

SEMESTER VII

Course Code: 23EVT701		Course Title: ASIC Design	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course aims to provide students with HDL coding, synthesize HDL constructs, understand RTL synthesis Flow, perform Static Timing Analysis for ASIC, provide detailed insight on physical design and its importance in design verification

Module I **22 Hours**

INTRODUCTION TO ASICS, CMOS LOGIC, AND ASIC LIBRARY DESIGN: Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort. **PARTITIONING, FLOORPLANNING AND PLACEMENT:** Floor Planning Goals and Floor planning tools, I/O and Power planning, Clock planning, Placement Algorithms. Pin Assignment Objectives, Measurement of Delay in floor planning.

Module II **23 Hours**

ROUTING, CLOCK DESIGN AND PHYSICAL VERIFICATION: Routing: Global routing, Detailed routing, Special routing, Clock Design, Clock Network Synthesis. Power and Ground Routing, Watchdog Timer, DRC, RC Extraction, Antenna Effect. **Physical verification:** Packaging- Layout Issues-Preventing electrical overstress, Static verification techniques-post-layout design verification

STATIC TIMING ANALYSIS: Timing Paths, Time borrowing, Basic concepts of Setup Time and Hold Time, Setup and Hold Violation, Delay – Timing path delay, Interconnect Delay models, Wire load model, Maximum clock frequency, Timing Models, SDF, SDC, Design Constraints- Transition Time, Fanout, Process Variation, Parasitic Extraction

SOCIAL, ENVIRONMENTAL AND ETHICAL ASPECTS:

Low-power and thermal-aware design – ESD protection – Design reliability – IP and reuse ethics – ASICs in safety-critical systems – Environmental impact and e-waste.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Analyze digital circuit delays using the logical effort technique to optimize performance within various implementation platforms, including FPGA architectures.	Analyze
CO2: Design fundamental logic cells and I/O cells for digital circuit implementation.	Apply
CO 3: Analyze the architectural resources and configurable logic blocks of modern FPGAs to evaluate their suitability for specific design requirements.	Analyze
CO 4: Apply algorithms for physical design, including floor planning, cell placement, and routing, to optimize digital circuit performance (length and speed).	Apply
CO5: Analyze the societal, environmental, and ethical aspects of ASIC design in professional engineering contexts.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO2	-	-	3	-	-	-	-	-	-	-	-	-	3	3
CO3	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO5	-	3	-	-	-	3	3	3	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Vaibbhav Taraate, ASIC Design and Synthesis RTL Design Using Verilog, Springer, Firs Edition, 2021, Singapore.

Reference Book(s):

R1 Khosrow Golshan, PHYSICAL DESIGN ESSENTIALS an ASIC Design Implementation Perspective, First Edition, 2010.

R2 Michael John Sebastian Smith, Application-Specific Integrated Circuits, First Edition, 2002.

R3 J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs, Springer, First Edition, 2010, USA.

Web References:

1. www.vlsi.wpi.edu/cds/explanations/lvs.html
2. http://www.eng.auburn.edu/
3. http://www.geoffknagge.com/fyp/index.shtml#asic

Course Code:23EVT702		Course Title: Verification and Testing	
Course Category: Major Course		Level: Higher	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

To provide foundational knowledge and practical skills in VLSI testing, including fault modeling, ATPG, and DFT techniques, for effective testing of combinational, sequential, and memory circuits in modern VLSI systems.

Module I **22 Hours**

FAULT MODELING: Physical faults and their modelling. Fault equivalence and dominance; fault collapsing, Fault simulation: parallel, deductive and concurrent techniques; critical path tracing. **TEST PATTERN GENERATION:** Test generation for combinational circuits: Boolean difference, D-algorithm, Podem, random etc. Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage.

DELAY FAULTS AND TEST PATTERN GENERATION: Delay faults and hazards; test pattern generation techniques, ATPG and its different types. Test pattern generation for sequential circuits: ad-hoc and structures techniques scan path and LSSD, boundary scan

Module II **23 Hours**

DESIGN FOR TESTABILITY: Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built- in Self-Test – Random Logic Bist – DFT for Other Test Objectives**.**

BIST: Built-in self-test techniques: LBIST and MBIST. Verification: logic level (combinational and sequential circuits), RTL-level (data path and control path). Verification of embedded systems. Use of formal techniques: decision diagrams, logic-based approaches. ASIC/IP Verification, direct and random testing, Error detection and correction codes.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Demonstrate the application of fault modeling and test pattern generation techniques to detect and analyze faults in combinational digital circuits.	Apply
CO 2: Examine delay faults and ATPG techniques in sequential circuits using scan-based DFT methods.	Analyze
CO 3: Implement scan and BIST techniques to improve the testability of digital circuits.	Apply
CO 4: Analyze BIST methods and verification techniques for digital and embedded systems using formal and simulation-based approaches.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	3	-	-	-	3	3	-	-	3	3
CO2	-	3	-	-	3	-	-	-	3	3	-	-	3	3
CO3	3	-	-	-	3	-	-	-	3	3	-	-	3	3
CO4	-	3	-	-	3	-	-	-	3	3	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer New York, 1st Edition, 2000. ISBN (Softcover): 978-1-4757-8142-7

T2. P. K. Lala, VLSI Testing: Digital and Mixed Analogue-Digital Techniques, Wiley-Interscience, 1998, ISBN-13: 978-0471164227, ISBN-10: 0471164228.

T3. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing, Kluwer Academic Publishers, 1st Edition, 2004.

Reference Book(s):

R1. P. K. Lala, Testing of Digital Systems, Wiley-Interscience, 1996, ISBN-13: 978-0471164289, ISBN-10: 0471164287.

R2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, Wiley-IEEE Press, 1st Edition, 1994.

R3. Niraj K. Jha, Sandeep Gupta, Testing of Digital Systems, Cambridge University Press, 1st Edition, 2003.

Web References:

1. https://onlinecourses.nptel.ac.in/noc20_ee76/preview

Course Code: 23EVL701		Course Title: Verification and Testing Lab	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 0: 0: 3	Credits:1.5	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is to develop hands-on skills in functional and structural verification using System Verilog and verification IPs through simulation environments.

List of Experiments: **45 Hours**

1. Fault Simulation and Test generation for combination circuits
2. Clock and reset rule check at RTL
3. Scan Chain Insertion, DRC and ATPG
4. At-Speed Patterns and On-Chip Clock Controllers (LoS and LoC)
5. SDF annotated simulation
6. Boundary scan test
7. Testing of memories (BIST insertion, validation and BIST repair)
8. Power-Aware Test Pattern Generation and Analysis
9. Fault Diagnosis and Localization
10. Design for Testability (DFT) Architecture Exploration and Implementation

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Generate and Assess Digital Test Patterns for Combinational and Sequential Circuit	Apply
CO2: Implement and Evaluate Design-for-Testability (DFT) Methodologies.	Apply
CO3: Execute and Interpret Pre- and Post-Layout Test Verification Simulations.	Apply
CO4. Diagnose and Prioritize Faults within Digital Circuits.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	1	-	-	-	-	-	-	1	3	3
CO2	3	-	-	-	1	-	-	-	-	-	-	1	3	3
CO3	3	-	-	-	1	-	-	-	-	-	-	1	3	3
CO4	3	-	-	-	1	-	-	-	-	-	-	1	3	3

High-3; Medium-2; Low-1

Reference Book(s):

R1. Laboratory Manual Prepared by Faculty of EE(VLSI) Dr. Mahalingam College of Engineering and Technology

Course Code:23EVP701		Course Title: Project Phase - I	
Course Category: Project		Course Level: Advanced	
L:T:P (Hours/Week) 0: 0: 8	Credits: 4	Total Contact Hours: 120	Max. Marks:100

Course Objectives:

To foster students' ability to recognize engineering challenges in the electronics domain and conceptualise innovative solutions through systematic research and preliminary development.

Module I **60 Hours**

Problem formulation and domain exploration: - Investigating contemporary challenges in electronics engineering - Background study and gap analysis through literature review of existing solutions - Project specification and boundary definition with clear deliverables and constraints - Resource planning and technical assessment evaluating infrastructure and implementation viability - Timeline development with structured schedule and measurable milestones - Conceptual design and system modeling through schematic representations and functional diagrams - Technology selection: choosing suitable platforms and development environments - Approach formulation establishing systematic methodology for solution development - Prototype development implementing core functionalities with basic performance verification - Progress documentation maintaining academic standards and citation protocols - Technical presentation communicating project status to evaluation panel.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply systematic research methodologies and literature review techniques to identify engineering problems and analyze existing solutions in electronics domain.	Apply
CO 2: Apply project planning and management tools to develop structured timelines, resource allocation, and milestone-based project execution strategies.	Analyze
CO 3: Evaluate technical requirements, design constraints, and feasibility factors to justify problem statement formulation and assess project scope viability.	Evaluate
CO 4: Create conceptual system architectures, design models, and implementation methodologies by synthesizing appropriate technological approaches for prototype development.	Create

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3		-	-	-	1	1	-	-	-	-	-	3	3
CO2	-	3	-	-	-	-	-	-	-	-	1	-	3	3
CO3	-	-	3	-	-	-	-	-	-	-	-	-	3	3
CO4	-	-	-	3	2	-	-	1	1	3	-	1	3	3

High-3; Medium-2;Low-1

SEMESTER VIII

Course Code:23EVP801		Course Title: Project Phase-II	
Course Category: Project		Course Level: Advanced	
L:T:P (Hours/Week) 0: 0: 12	Credits: 6	Total Contact Hours:240	Max. Marks:200

Course Objectives:

To enable students to execute comprehensive engineering solutions through systematic implementation, rigorous testing, and professional documentation while developing industry-ready technical communication and project management skills.

Module I **60 Hours**

Objective refinement and final specification consolidating project requirements based on practical considerations and societal impact - End-to-end solution realization implementing complete functional system using selected hardware/software platforms and methodologies –

Full-scale development and integration executing comprehensive system build through appropriate engineering processes including design, coding, assembly, or fabrication - Comprehensive testing and performance validation conducting systematic evaluation through experimental procedures, data analysis, and measurement protocols –

System characterization and benchmarking assessing solution effectiveness using standard engineering parameters and comparative analysis - Iterative refinement and enhancement implementing design modifications based on evaluation outcomes to

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply comprehensive engineering design principles and implementation methodologies to develop complete functional solutions addressing identified problems.	Apply
CO 2: Apply systematic testing protocols, validation procedures, and performance measurement techniques to evaluate and optimize developed solutions.	Apply
CO 3: Evaluate experimental results, performance data, and system effectiveness against established criteria to assess solution quality and make design improvement decisions.	Evaluate
CO 4: Create comprehensive technical documentation, professional reports, and presentation materials that effectively communicate engineering solutions and project outcomes to stakeholders.	Create

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	1	1	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	1	-	3	3
CO3	-	-	3	-	-	-	-	-	-	-	-	-	3	3
CO4	-	-	-	3	2	-	-	1	1	3	-	1	3	3

High-3; Medium-2;Low-1

DIVERSIFIED

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course Code: 23ECE051		Course Title: Computer Architecture (Common to EA,EC,EV)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to impart knowledge on memory organization, addressing modes of a processor, the organization of cache memory and pipelining techniques for the design of high speed processor.

Module I **22 Hours**

Basic Structure of Computers:

Evolution of Microprocessor - Basic Processor Architecture - Operational concepts – Performance.

Instruction Set Architecture:

Memory location - Memory Operations – Instructions and sequencing - Addressing modes - CISC Vs RISC.

Basic Input/Output, Processing Unit :

Accessing I/O devices - Interrupts -Buses - Instruction Execution-DMA–Hardware Components – Instruction Fetch and Execution Steps – Control Signals-Hardwired Control - CISC Style Processors: Interconnect using Buses, Micro programmed Control.

Module II **23 Hours**

The Memory System: Characteristics of Memory Systems - Cache Memory Principles - Elements of Cache Design - Mapping Function - Example of Mapping Techniques - Replacement Algorithms - Performance Consideration.

Pipelining : Basic concept - Pipeline Organization and issues - Data Dependencies – Memory Delays – Branch Delays – Resource Limitations - Performance Evaluation - Superscalar operation –Pipelining in CISC Processors - Instruction Level Parallelism – Parallel Processing Challenges – Flynn’s Classification – Hardware multithreading – Multicore Processors: GPU, Multiprocessor Network Topologies.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the features of different instruction set architectures to evaluate their effect on system performance in real-world scenarios.	Apply
CO 2: Analyze various design elements to determine suitable memory organization for optimized performance.	Analyze
CO 3 : Examine the principles of pipelining and instruction-level parallelism to understand their impact on processor performance.	Analyze
CO 4: Independently learn about emerging computer architectures and deliver an oral presentation highlighting their impact on society and their contribution to sustainable and environmentally friendly technologies.(For Internal Assessment only)	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-		-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-	2	-
CO4	-	-	-	-	-	2	2	-	1	1	-	2	2	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Carl Hamacher, Zvonok Vranesic, Safwat Zaky, Naraig Manjikian, “Computer Organization and Embedded Systems”, 6th Edition, McGraw Hill, 2012

T2. David A. Patterson and John L. Hennessey, “Computer Organization and Design: The Hardware/Software Interface”, 5th Edition, Morgan Kauffman / Elsevier, 2014

Reference Book(s):

R1. William Stallings, “Computer Organization and Architecture: Designing for Performance”, 10th Edition, Pearson Education, 2016

R2. John L. Hennessey and David A. Patterson, “Computer Architecture: A Quantitative Approach”, Morgan Kauffman / Elsevier, 5th edition, 2012

Web References:

1. https://www.coursera.org/lecture/comparch/course-introduction-Ouq7L
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-823-computer-system-architecture-fall-2005/index.html
3. http://www.nptel.ac.in/courses/106102062/

Course Code: 23EEE014		Course Title: Industrial Automation (Common to EA,EC,EE,EV)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to cutting-edge technologies such as Programmable Logic Controllers (PLC), Supervisory Control and Data Acquisition (SCADA), and Distributed Control Systems (DCS), students will learn to develop innovative automation solutions. The course emphasizes hands-on experience in designing control logic programs, configuring industrial networks, and exploring real-world applications.

Module I **22 Hours**

Introduction to Factory Automation: History and developments in industrial automation- Vertical integration of industrial automation- Building blocks in Automation: Processing systems, Multi microprocessor systems, LAN, analog and digital I/O modules, remote terminal unit

Programmable Logic Controllers :PLC an Overview- Parts and Architecture of PLC- Principles of Operation - I /O Specifications - Memory types-Programming devices- PLC vs Computers, PLC size and Applications, Advantages of PLC, selection of PLC

Programming of PLC : Program scan - PLC Programming Languages-Simple process control programs using Relay Ladder Logic - Programming Timers : On delay timer, OFF delay timer- Programming counters: Up and Down counter – PLC arithmetic functions – Program Control Instructions-Math Instructions-data transfer operations-Data comparison instructions

Module II **23 Hours**

Industry Networking and SCADA :PLC Networking- Networking standards & IEEE Standard - Protocols - Field bus - Process bus and Ethernet .SCADA-Channel scanning-conversion to engineering units- data processing –Distributed SCADA systems- HMI introduction

Distributed Control System and Applications : DCS: Evolution – Different architectures – local control unit – Operator interface – Displays – Engineering interface. Applications: Thermal power plant-cement plant-water treatment plant- Solar, windmill substation automation.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the principles of automation to identify its necessity in industrial processes.	Apply
CO 2: Analyze the architecture and types of PLCs used in industrial automation to select suitable options.	Analyze
CO 3 : Develop PLC-based control logic programs to meet specific industrial requirements.	Apply
CO 4: Analyze industrial networking protocols and SCADA systems to implement effective automation.	Analyze
CO 5: Apply the concepts of DCS to evaluate its applications in power plants and other industrial setups.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	3	-	-	-	-	-	-	-	3	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO5	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Frank D Petruzella “Programmable Logic Controllers", McGraw Hill Education India Private Limited, 6th Edition, 2023.

T2. Bolton.W, “Mechatronics”, Pearson Education, Delhi, 7th Edition,2018.

Reference Book(s):

R1. John W Webb & Ronald A Reis, “Programmable logic controllers: Principles and Applications”, Prentice Hall India, 5th edition, 2011

R2. Dobrivojie Popovic, Vijay P. Bhatkar,“ Distributed Computer Control for Industrial Automation”, Marcel Dekkar Inc., New York, 1st edition, 2011.

R3. Krishna Kant, „Computer based Industrial Control", Prentice Hall of India, 2nd edition, 2010

R4. Rajesh Mehra and Vikrant Vij, “PLCs& SCADA- Theory and Practice”, Laxmi Publications, 1st edition, 2019.

Web References:

1.http://www.fieldbus.org

2.www.nptel.ac.in/downloads/108105063/

3.http://nptel.ac.in/courses/108105062/18

Course Code: 23EEE085		Course Title: Automotive Electronics (Common to EA,EC,EE,EV)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The learners will be able to develop foundational knowledge of mechanical and electronic systems in modern automobiles. Additionally, the course focus on the role and implementation of embedded systems and X-by-wire technologies in automotive applications.

Module I **22 Hours**

Automotive Mechanical Systems: Overview of vehicle systems including the powertrain (air, fuel, ignition, exhaust and cooling), transmission types, braking systems, and steering mechanisms.

Electronics in Automotive Systems: Role of electronics in enhancing performance, control and compliance with legislation. Introduction to chassis subsystems (ABS, TCS, ESP), and comfort/safety features (airbags, seatbelt tensioners, cruise control).

Module II **23 Hours**

Drive-By-Wire Technologies: X-by-wire technologies: Steer-by-wire, brake-by-wire, shift-by-wire, and future trends.

Embedded Systems and EV Introduction: Sensor and actuator systems in gasoline/diesel engines (NOx, knock, MAP, oxygen, throttle position), thermal actuators, and body electronics (central locking, climate control). Introduction to electric vehicle classifications.

Vehicle Communication Protocols: Overview of SPI, I2C and automotive-specific protocols including CAN, LIN and MOST. Introduction to AUTOSAR framework for standardization and Ethernet.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Identify the key components and functions of automotive mechanical systems such as powertrain, transmission, braking, and steering, safety, and compliance.	Apply
CO2: Apply the role of electronic systems in enhancing vehicle performance, safety features, and regulatory compliance.	Apply
CO3: Examine the working principles of X-by-wire technologies and apply knowledge of sensors and actuators in automotive embedded system design.	Apply
CO4: Apply standard in-vehicle communication protocols to develop basic automotive communication systems and demonstrate the use of AUTOSAR for system integration.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO4	3	-	-	-	-	-	-	-	1	1	-	-	1	-

High-3; Medium-2;Low-1

Textbooks:

T1. Robert Bosch GmbH, "Bosch Automotive Handbook", 10th Edition, Wiley Publishers, 2019.

T2. William B. Ribbens, “Understanding Automotive Electronics”, 7th Edition, SAMS/Elsevier Publishing, 2012

Reference Book(s):

R1. Robert Bosch Gmbh, Automotive Electrics and Automotive Electronics, Systems and Components, Networking and Hybrid drive, 5th edition, Springer Vieweg, Wiesbaden 2014

R2. Knowles.D, Automotive Electronic and Computer Controlled Ignition Systems, Reston Pub Co,1990 R3. Denton.T , Automobile Electrical and Electronic Systems: Automotive Technology: Vehicle Maintenance and Repair, 2012

Web References:

1. www.austincc.edu/autotech
2. https://acconline.austincc.edu/webapps/portal/frameset.jsp

Course Code:23MEE008		Course Title: PLM for Engineers (Common to all Programmes)	
Course Category: Minor		Course Level: Higher	
L:T:P(Hours/Week) 2:0 : 2	Credits:3	Total Contact Hours: 60	Max Marks:100

Course Objectives:

The course is intended to apply Product Lifecycle Management (PLM) fundamentals and principles to develop strategies, manage product lifecycles, optimize engineering processes, configure Bills of Materials, and leverage digital manufacturing environments for practical applications and customer-centric use cases.

Module I **22 Hours**

Business Strategy in the PLM

Definition, PLM Lifecycle Model, Threads of PLM, Need for PLM, Opportunities and Benefits of PLM, Components and Phases of PLM, PLM feasibility Study, PLM Visioning, Strategy, Impact of strategy, implementing a PLM strategy, PLM Initiatives to Support Corporate Objectives, Infrastructure Assessment.

Business Processes in the PLM and Product Development Concepts

Characteristics of PLM, Environment Driving PLM, PLM Elements, Drivers of PLM, Conceptualization, Design, Development, Validation, Production, Support of PLM. Engineering Vaulting, Product Reuse, Smart Parts, Engineering Change Management, Workflow Management. Bill of Materials (E-BOM, M-BOM, S-BOM) and Process Consistency, Product Structure, Configuring BOM

Module II **23 Hours**

Digital Mock Up and Validation

Simulation Process Management, Variant Management, Digital Mock-Up and Prototype Development, Design for Environment, Virtual Testing and Validation, Marketing Collateral

Digital Manufacturing in the PLM

Digital Manufacturing, Benefits of Digital Manufacturing, Manufacturing the First-One, Ramp Up, Virtual Learning Curve, Manufacturing the Rest, Production Planning.

Customer Use Cases of the PLM

Impact and Challenges faced while implementing a successful PLM strategy -Rolls Royce, Nissan Motor, Sunseeker International , Xtrac ,kesslers international and monier and weatherford international.

List of Experiments: **15 Hours**

1. Demonstrate the 2-Tier & 4-Tier Architectures and Basic Team center applications like Organization, Project, and Schedule Manager.
2. Create CAD and Non-CAD datasets (MS Office, Notepad, etc.) by using explicit and implicit Check-In and Check-Out to create multiple iterations
3. Create the access control (Read, Write, and Delete) for the given dataset and block the access rights to other group members belongs to the same department. Also Perform the Impact Analysis (Where Used and Where Referenced) of a given dataset which is used in multiple assemblies.
4. Create the Product Structure in Structure Manager with 5 components assembled in first level and 3 components Assembled in second, third and fourth level with the sub-assemblies and export the assembly in local drive. Also, demonstrate the Variant Management.
5. Export the CAD dataset as a JT file and perform the various visualization tasks like Measurements, Sectioning, PMI, and Mark-up using JT2GO application

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO 1: Apply the fundamentals of PLM principles to develop a PLM strategy for a system.	Apply
CO 2: Apply PLM principles to manage product lifecycles, optimize engineering processes, and configure Bill of Materials with consistent workflows	Apply
CO 3 : Apply the Digital Manufacturing environment using PLM for use cases.	Apply
CO 4: Develop and present a report individually by applying various modules of PLM software for an engineering project.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	3	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	1	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	-	-	3	-	-	-	-	-	1	1	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. John Stark, “Product Lifecycle Management: Volume 1: 21st Century Paradigm for Product Realisation”, Springer International Publishing Switzerland, 4th edition, 2020.

T2. Grieves Michael, “Product Lifecycle Management- Driving the Next Generation of Lean Thinking”, McGraw-Hill, 2010.

T3. Wang, Lihui; Nee, Andrew Y.C. (Eds.) Collaborative Design and Planning for Digital Manufacturing, Springer, 2009.

Reference Book(s):

R1. Elangovan, U., “Product Lifecycle Management (PLM)”. Boca Raton, CRC Press, 2020.

R2. Fabio Giudice, Guido La Rosa, Product Design for the environment-A life cycle approach, Taylor & Francis 2006.

R3. Antti Saaksvuori, “ Product Life Cycle Management” - Anselmi Immonen, Springer, 3rd Edition, 2008.

Course Code:23MEE030		Course Title: Principles of Management (Common to EA,EC,EE,EV,ME)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

This course is intended to study the role of managers, the significance of planning, decision-making, and strategies in international business, the importance of organizing tasks, various motivational theories, and control techniques.

Module I **22 Hours**

OVERVIEW OF MANAGEMENT :

Organization – Management – Role of managers – Evolution of Management thought – Organization and the environmental factors – Managing globally – Strategies for International Business

PLANNING:

Nature and Purpose planning – Planning process – Types of Plans – Objectives – Managing by Objective (MBO) Strategies – Types of strategies – Policies – Decision Making – Types of decision – Decision Making Process – Rational Decision Making Process – Decision Making under different Conditions.

ORGANISING:

Nature and purpose of organizing – Organization structure – Formal and informal groups organization – Line and Staff authority – Departmentation – Span of Control – Centralization and Decentralization – Delegation of authority – Staffing – Selection and Recuritment – Orientation Career Development – Career stages – Training – Performance appraisal.

Module II **23 Hours**

DIRECTING :

Creativity and Innovation – Motivation and Satisfaction – Motivation Theories Leadership – Leadership theories – Communication – Hurdles to effective communication – organization culture – elements and types of culture – managing cultural diversity.

CONTROLLING:

Process of controlling – types of control – budgetary and non – budgetary control techniques – managing productivity – cost control – purchase control – maintenance control – quality control – planning operations.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply management principles to understand the roles and functions of managers in various organizational and business contexts.	Apply
CO 2: Develop and implement effective planning, decision-making, and strategic management practices to achieve organizational objectives in both domestic and international settings.	Apply
CO 3 : Prepare and present a seminar individually on organizational, motivational and control techniques including task allocation, employee engagement strategies, budgeting, and quality management to enhance productivity and efficiency.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	2	2	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. hen P. Robbins, Rolf Bergman and Mary Coulter, “Management”, Prentice Hall of India, 8th edition, 2017.

T2. Charles W.L Hill, Steven L McShane, “Principles of Management”, Mcgraw Hill Education, 2008

Reference Book(s):

R1. Hellriegel, Slocum & Jackson, “Management – A Competency Based Approach”, Thomson South Western, 10th edition, 2007.

R2. Harold Koontz, Heinz Weihrich and mark V Cannice, “Management – A global & Entrepreneurial Perspective”, Tata McGraw Hill, 12th edition, 2007.

R3. Andrew J. Dubrin, “Essentials of Management”, Thomson Southwestern, 7th edition, 2007

Course Code: 23SCE050		Course Title: Cyber security	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Pre-requisites

- Nil

Course Objectives: To provide foundational knowledge of cyberspace, cyber laws, and digital security practices to identify, prevent, and respond to cyber threats.

Module I **22 Hours**

Introduction to Cyber Security: Defining Cyberspace - Overview of Computer and Web-technology - Architecture of cyberspace, Internet, World wide web, Advent of internet, Internet infrastructure for data transfer and governance, Internet society, Regulation of cyberspace, Concept of cyber security, Issues and challenges of cyber security.

Cyber-crime and Cyber law: Classification of cyber-crimes - cyber-crime targeting computers and mobiles, cyber-crime against women and children, financial frauds, social engineering attacks, malware and ransomware attacks, zero day and zero click attacks, Cybercriminals modus-operandi , Reporting of cyber-crimes, Remedial and mitigation measures, Legal perspective of cyber-crime, IT Act 2000 and its amendments, Cyber-crime and offences, Organizations dealing with Cyber-crime and Cyber security in India, Case studies

Module II **23 Hours**

Social media and Security: Introduction to Social networks, Social media – Types, platforms, monitoring, Hashtag, Viral content, marketing, Challenges, opportunities and pitfalls in online social network, Security issues related to social media, Flagging and reporting of inappropriate content, Laws regarding posting of inappropriate content, Best practices for the use of Social media, Case studies.

E-Commerce and Digital Payments: E- Commerce - Definition, Components, Security, Threats, Best practices - Digital payments – Components, stake holders, Modes of digital payments - Banking Cards, Unified Payment Interface (UPI), e-Wallets, Unstructured Supplementary Service Data (USSD), Aadhar enabled payments, Digital payments related common frauds and preventive measures. RBI guidelines on digital payments and customer protection in unauthorised banking transactions. Relevant provisions of Payment Settlement Act,2007.

Digital Devices Security, Tools and Technologies for Cyber Security: End Point device and Mobile phone security, Password policy, Security patch management, Data backup, Downloading and management of third party software, Device security policy, Cyber Security best practices, Significance of host firewall and Ant-virus, Management of host firewall and Anti-virus, Wi-Fi security, Configuration of basic security policy and permissions

Case studies and Assignments:

1. Prepare checklist for following scenarios :
   a) Reporting cybercrime at Cybercrime Police Station.
   b) Reporting cybercrime online.
   c) Using popular social media platforms.
   d) Secure net banking.
2. Demonstrate the following:
   a) Reporting phishing emails, email phishing attack and preventive measures
   b) Reporting and redressal mechanism for violations and misuse of Social media platforms.
3. Manage the following activities:
   a) Privacy and security settings for popular Social media platforms, Mobile Walletsand UPIs.
   b) Application permissions in mobile phone.
4. Perform the following activities:
   a) Setting, configuring and managing three password policy in the computer(BIOS, Administrator and Standard User).
   b) Setting and configuring two factor authentication in the Mobile
5. Demonstrate the following:
   a) Security patch management and updates in computer and mobiles.
   b) Wi-Fi security management in computer and mobile.
6. Install and configure computer Anti-virus & Computer Host Firewall.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Design appropriate checklists and procedures for secure cyber practices and effective response to cybercrime incidents across various platforms.	Apply
CO2: Illustrate the functioning of cyberspace infrastructure and demonstrate how regulatory frameworks address cyber threats.	Apply
CO3: Analyze privacy and security configurations in social media platforms and digital applications to identify potential risks and propose suitable mitigation strategies.	Analyze
CO4: Apply evolving cybersecurity tools and device protection practices through continuous learning to address emerging digital security challenges.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	3	-	-	2	-	-	2	2	-	-		
CO2	3	-	-	-	-	-	-	-	-	-	-	-		
CO3	-	2	-	-	2	-	-	1	2	2	-	-		
CO4	3	-	-	-	2	-	-	-	-	-	-	2		

High-3; Medium-2;Low-1

Text Book(s):

T1. Cyber Crime Impact in the New Millennium, R. C Mishra. Auther Press. 2010.

T2. Cyber Security Understanding Cyber Crimes, Computer Forensics and Legal Perspectives by Sumit Belapure and Nina Godbole, 1st Edition, Wiley India Pvt. Ltd, 2011.

T3. Security in the Digital Age: Social Media Security Threats and Vulnerabilities by Henry A. Oliver, Create Space Independent Publishing Platform, PearsonEducation, 2001.

Reference Book(s):

R1. Network Security Bible, Eric Cole, Ronald Krutz, James W. Conley, 2nd Edition, Wiley India Pvt. Ltd, 2001

R2. Security Fundamentals of Network by E. Maiwald, McGraw Hill ,2014

R3. Cyber Laws: Intellectual Property & E-Commerce Security by Kumar K,Dominant Publishers, 2011.

Web References:

1. https://unacademy.com/content/upsc/study-material/science-and-technology/initiatives-taken-by-indian-government-for-cyber-security/
2. https://cybercrime.gov.in/
3. https://www.meity.gov.in/cyber-security-division
4. https://intellipaat.com/blog/what-is-cyber-security/

Course Code: 23AUE050		Course Title: Entrepreneurship Development (Common to all Programmes)	
Course Category: Minor		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to develop entrepreneurial mindset and skills by identifying and validating problems through human-centered design, analyzing markets and customers to create value propositions and MVPs, exploring business models with financial and feasibility analysis, and preparing investible pitch decks to attract stakeholders

Module I **22 Hours**

Entrepreneurial Mindset

Introduction to Entrepreneurship: Definition – Types of Entrepreneurs – Emerging Economics – Developing and Understanding an Entrepreneurial Mindset – Importance of Technology Entrepreneurship – Benefits to the Society.

Opportunities

Problems and Opportunities – Ideas and Opportunities – Identifying problems in society – Creation of opportunities – Exploring Market Types – Estimating the Market Size, - Knowing the Customer and Consumer - Customer Segmentation - Identifying niche markets – Customer discovery and validation; Market research techniques, tools for validation of ideas and opportunities

Activity Session: Identify emerging sectors / potential opportunities in existing markets - Customer Interviews: Conduct preliminary interviews with potential customers for Opportunity Validation - Analyse feedback to refine the opportunity.

Prototyping & Iteration

Prototyping – Importance in entrepreneurial process – Types of Prototypes - Different methods – Tools & Techniques. Hands-on sessions on prototyping tools (3D printing, electronics, software), Develop a prototype based on identified opportunities; Receive feedback and iterate on the prototypes.

Module II **23 Hours**

Business models & pitching

Business Model and Types - Lean Approach - 9 block Lean Canvas Model - Riskiest assumptions to Business Models – Using Business Model Canvas as a Tool – Pitching Techniques: Importance of pitching - Types of pitches - crafting a compelling pitch – pitch presentation skills - using storytelling to gain investor/customer attention.

Activity Session: Develop a business model canvas for the prototype; present and receive feedback from peers and mentors - Prepare and practice pitching the business ideas- Participate in a Pitching Competition and present to a panel of judges - receive & reflect feedback

Entrepreneurial Ecosystem

Understanding the Entrepreneurial Ecosystem – Components: Angels, Venture Capitalists, Maker Spaces, Incubators, Accelerators, Investors. Financing models – equity, debt, crowdfunding, etc, Support from the government and corporates. Navigating Ecosystem Support: Searching & Identifying the Right Ecosystem Partner – Leveraging the Ecosystem - Building the right stakeholder network

Activity Session: Arrangement of Guest Speaker Sessions by successful entrepreneurs and entrepreneurial ecosystem leaders (incubation managers; angels; etc), Visit one or two entrepreneurial ecosystem players (Travel and visit a research park or incubator or makerspace or interact with startup founders).

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Apply entrepreneurial mindset principles to identify societal problems and transform them into viable business opportunities.	Apply
CO2: Develop prototypes using suitable tools and techniques for the validated opportunities through iterative processes.	Apply
CO3: Demonstrate a Business Model Canvas using the Lean approach and pitch the startup idea effectively using storytelling and presentation skills.	Apply
CO4: Analyze customer segments, market size, and niche markets to validate entrepreneurial opportunities through market research and customer interviews.	Analyze
CO5: Evaluate the role and components of the entrepreneurial ecosystem to identify and engage the right ecosystem partners and funding models for startup success.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	1	-	-	-	-	-	-	-	-
CO2	-	-	3	-	1	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	1	1	-	-	-	-
CO4	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO5	-	-	-	2	-	-	-	-	-	-	1	1	-	-

High-3; Medium-2;Low-1

Reference Book(s):

T1. Robert D. Hisrich, Michael P. Peters, Dean A. Shepherd, Sabyasachi Sinha Entrepreneurship, McGrawHill, 11th Edition,2020.

T2. Ries, E. The Lean Startup: How Today's Entrepreneurs Use Continuous Innovation to Create Radically Successful Businesses. Crown Business,2011.

T3. Blank, S. G., & Dorf, B. The Startup Owner's Manual: The Step-by-Step Guide for Building a Great Company. K&S Ranch.2012.

T4. Roy, R. Indian Entrepreneurship: Theory and Practice. New Delhi: Oxford University Press,2017.

T5. Osterwalder, A., & Pigneur, Y. Business Model Generation: A Handbook for Visionaries, Game Changers, and Challengers. John Wiley & Sons,2010.

Course Code: 23AUE051		Course Title: Design Thinking and Innovation (Common to all Programmes)	
Course Category: Major		Course Level: Practice	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to equip learners with practical skills in design thinking, empathy, prototyping, testing, and implementation for user-centered innovation and effective product development.

Module I **17+6 Hours**

Introduction- Importance of Design Thinking, Human Centered Design, Six-Step Design Thinking Process-Framework for Innovation-DT-a nonlinear process.

Empathy-importance of empathy in design thinking- empathy vs sympathy- steps of empathize-understanding customer needs-empathy methods and tools-empathy map-5W 1H framework-empathize in UX/UI Design-users Interview

Module II **18+4 Hours**

Prototype: Introduction to Proof of concept-MVP-Prototype and its types-prototype methodology- innovation and its types-Tools for prototyping: concept sketching/CAD/3D Printing.

Testing: Importance of testing in product development-design validation-market analysis: TAM-SAM-SOM-EVG.

Implementation - redesign of solution and iterative process.

List of activities

Core Stream

Empathy

1. What challenges does the user face daily commuting to work place?
2. What are the user's biggest frustrations when interacting with vehicle maintenance engineer?
3. Understand the user for building old age home.

Define

1. A construction site supervisor needs better real-time communication tools because delayed updates cause safety risks. (Provide the empathy data)
2. "Drivers get confused by inconsistent road signs," create: "How might we improve road sign clarity to reduce driver confusion?"
3. A daily commuter needs a safer way to cross busy intersections because current pedestrian signals are confusing and slow. (Provide the empathy data)

Ideate

1. Develop a creativity safer vehicle dashboard design
2. Develop an improved road drainage system
3. Design an innovative solution to reduce urban flooding caused by heavy rains.
4. Design a Hybrid engine designs incorporating solar panels on the car roof.

Prototype

1. Prototype development (both low fidelity and high fidelity) on any real world problem

IT and Circuit Stream:

Activity 1:

Students role-play as designers and users- create an empathy map with 4 quadrants: *Says, Thinks, Does, Feels*

Circuit Stream- Empathy Interview and Persona Creation

Define- development of problem Statement-Elements of a Good Problem Statement-Tools: Point-of-View (POV) Statements-How Might We (HMW) Questions-User Personas.

Ideation in Design Thinking-Importance of Ideation-Metrics of ideation -tools: Brainstorming-Mind Mapping-SWOT.

Activity 2:

IT Stream- SWOT analysis on software project idea.

Circuit Stream -Idea Pitch Canvas using Brainstorming + Mind Mapping

Convert ideas into quick prototypes and validate through early testing.

Activity 3:

IT Stream -Build a simple algorithm to test feasibility- TAM-SAM-SOM market analysis chart

Circuit Stream -MVP Canvas and Concept Sketching

Circuit Stream -Iterative Redesign and Peer Testing Sprint

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply design thinking tools like empathy mapping, problem definition, and ideation to create user-centered innovative solutions.	Apply
CO2: Apply prototyping, innovation, testing, and iterative redesign techniques in product development and market analysis..	Apply
CO3: Apply design thinking to develop, prototype, and validate innovative engineering solutions in capstone projects for real-world applications.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	2	-	-	-	2			2	2	2	2	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Sabell Osann, Lena Mayer , Inga Wiele ,The Design Thinking Quick Start Guide: A 6-Step Process for Generating and Implementing Creative Solutions, Wiley, 2020.

T2. Christian Müller-Roterberg, Handbook of Design Thinking, Kindle Direct Publishing,2018.

Reference Book(s):

R1. Teun den Dekker, Design Thinking, Taylor & Francis, International edition, 2020.

R2. Kaushik Kumar, Divya Zindani, J.Paulo Davim, Design Thinking to Digital Thinking, Springer, 2019.

R3.S. Balaram, Thinking Design, SAGE Publications, 2011.

Course Code: 23ITE047		Course Title: Intellectual Property Rights (Common to all Programmes)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to learn the fundamental concepts of Intellectual Property Law, including patent classifications, trademark strategies, and copyright protections.

Module I **22 Hours**

Intellectual Property: An Introduction: Intellectual Property Law: Patent Law-Copyright Law-Trademark Law- Trade secret Law-Right of Publicity-Paralegal tasks in Intellectual Property Law-Ethical obligations of the paralegal in Intellectual Property Law-Trade secrets: Protectible as a trade secret-Maintaining trade secrets-Protecting an Idea.

Patents: Rights and Limitations: Sources of patent law-Subject matter of Patents: Utility Patents-Plant Patents-Design Patents- Design Patents and copyright-Design Patents and trademarks-Computer Software, Business methods and Patent Protection-Rights under Patent Law-Patent Requirements-Limitations on Patent Rights-Patent Ownership.

Module II ` **23 Hours**

Patents: Research, Applications, Disputes, and International Considerations: Patent Search Process-Patent Application Process-Patent Infringement-Patent Litigation, International Patent laws.

Principles of Trademark: Trademarks and Unfair Competition-Acquiring Trademark Rights-Types of Marks, Strong Marks Versus Weak Marks-Selecting and Evaluating a Trademark-International Trademark Laws.

Principles of Copyrights: Sources of Copyright Law- The Eight Categories of Works of Authorship-Derivative Works and Compilations- Rights and Limitations: Grant of Exclusive Rights–Copyrights Ownership- International Copyright Laws.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply the fundamental concepts of Intellectual Property Law to real- world scenarios.	Apply
CO2: Demonstrate an understanding of the Rights and Limitations of various patents through practical examples.	Apply
CO3: Analyze the process of patent searching and application filing to assess its effectiveness in protecting intellectual property.	Analyze
CO4: Examine the principles of trademark and copyright to differentiate their roles and implications in intellectual property law.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	-
CO2	-	-	-	2	-	-	-	-	-	-	-	-	-	2
CO3	-	3	-	-	2	-	-	-	-	2	-	-	-	-
CO4	-	2	-	-	3	-	-	3	2	-	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Richard Stim, “Intellectual Property: Copyrights, Trademark and Patents”, Cengage learning, 2nd edition 2012.

Reference Book(s):

R1. Deborah E. Bouchoux, “Intellectual Property: The Law of Trademarks, Copyrights, Patents and Trade Secrets”, Cengage Learning, 3rd Edition, 2013.

R2. Prabuddha Ganguli, “Intellectual Property Rights: Unleashing the Knowledge Economy”, McGraw Hill Education, 2017.

R3. David Llewelyn, Tanya Frances Aplin, “Intellectual Property Patents, Copyrights, Trademarks & Allied Rights”, Sweet & Maxwell, 2023.

R4. William F. Patry ,"Principles of Intellectual Property: Patents, Trademarks, and Copyrights", Wolters Kluwer, 2023.

Web References:

1. https://ipindia.gov.in/writereaddata/Portal/ev/sectionsindex.html

OPEN ELECTIVE

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course code: 23EVO001		Course Title: Microelectronics	
Course Category: Open Elective		Course level: Higher	
L: T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objective:
To provide a thorough understanding of semiconductor devices and their operation in analog circuit design and to develop analytical and design skills for building and evaluating electronic amplifiers using BJTs and MOSFETs.

Module I: Semiconductor Devices and Basic Amplifier Concepts 22 Hours

Semiconductor Fundamentals: Energy bands, charge carriers, drift, and diffusion current, p-n junction: I-V characteristics, small-signal model. **Diode Circuits:** Ideal diode model, piecewise-linear model, Rectifiers, clamping and clipping circuits, Zener diode voltage regulators

Bipolar Junction Transistor (BJT): BJT operation modes, characteristic curves, BJT models: DC and small-signal hybrid-π model, Biasing methods: fixed bias, voltage-divider bias, Load line and Q-point stability. **MOSFET Devices:** Structure and operation of enhancement-type NMOS and PMOS, Threshold voltage, I-V characteristics, modes of operation, DC analysis and biasing of MOSFETs

Module II: Amplifier Design and Frequency Response 23 Hours

Basic Amplifier Building Blocks: Concept of amplification, gain, input and output resistance, Small-signal operation and modeling, Common emitter and common source amplifiers. **Multistage Amplifiers:** Coupling methods (RC, direct, transformer) Cascading gain stages and loading effect, Level shifting and bias stabilization in multi-stage circuits.

Frequency Response of Amplifiers: Low-frequency and high-frequency analysis, Bode plots, poles, and zeros. Miller's Theorem and its application, Dominant pole approximation. **Feedback and Stability:** (Introductory) Concept of negative feedback in amplifiers, Effects on gain, input/output resistance, bandwidth, Types of feedback topologies (series-shunt, etc.)

Course Outcomes		Cognitive Level
At the end of this course, students will be able to:		
CO1:	Interpret the characteristics and operation of diodes, BJTs, and MOSFETs using appropriate models.	Apply
CO2:	Design biasing circuits for BJTs and MOSFETs to achieve desired operating points.	Apply
CO3:	Analyze single-stage and multi-stage transistor amplifiers for voltage gain and impedance.	Analyze
CO4:	Determine the frequency response of BJT and MOSFET amplifiers using small-signal equivalent models	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High = 3, Medium = 2, Low = 1

Text Book

T1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, 7th ed., New York, NY, USA: Oxford University Press, 2015.
T2. J. Millman and C. C. Halkias, Electronic Devices and Circuits, 2nd ed., New York, NY, USA: McGraw-Hill, 2008.
T3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., Upper Saddle River, NJ, USA: Pearson, 2013.

Reference Books

R1. D. A. Neamen, Microelectronics: Circuit Analysis and Design, 4th ed., New York, NY, USA: McGraw-Hill, 2010
R2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 7th ed., Boston, MA, USA: Pearson, 2014.
R3. M. H. Rashid, Microelectronic Circuits: Analysis and Design, 3rd ed., Boston, MA, USA: Cengage Learning, 2011.
R4. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed., Hoboken, NJ, USA: Wiley, 2009.

Web References

1. https://nptel.ac.in/courses/117102060
2. https://nptel.ac.in/courses/108105132
3. https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/

Course code: 23EVO002		Course Title: Nano Electronics	
Course Category: Open Elective		Course level: Higher	
L: T:P (Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objective:
To introduce the fundamental principles, materials, and device physics at the nanoscale and to develop the ability to analyze and apply nanoscale technologies in modern electronic devices.

Module I: Fundamentals of Nanoscience and Materials **22 Hours**

Introduction to Nanoscience and Nanotechnology: Evolution and scope, Top-down vs bottom-up approaches, Interdisciplinary nature, and applications. Quantum Effects at the Nanoscale. **Nanomaterials and Structures:** Carbon nanostructures: fullerenes, CNTs, graphene, Quantum dots, nanowires, nanorods, nanoshells, Metal and semiconductor nanoparticles

Synthesis Techniques: Physical methods: sputtering, evaporation, Chemical methods: sol-gel, CVD, hydrothermal, Self-assembly, and template-based growth. **Characterization Techniques:** SEM, TEM, AFM, XRD, Importance of scale, resolution, and surface analysis

Module II: Nanoelectronic Devices and Applications **23 Hours**

Nanoelectronic Devices: Device miniaturization and scaling limits, Short-channel effects in MOSFETs, Tunnel FETs, FinFETs, GAAFETs, Single Electron Transistors (SETs), Resonant Tunneling Diodes (RTDs). **Carbon-Based and Molecular Electronics:** CNT-FETs: structure, fabrication, operation, Graphene transistors: bandgap tuning and challenges, Molecular wires, and diodes.
Fabrication Techniques for Nanoscale Devices: Electron-beam lithography, nanoimprint lithography, Bottom-up device assembly techniques. **Applications and Future Trends:** Nano in sensors, memory, energy devices, and healthcare, Challenges in integration, reliability, and scaling, Ethical, safety, and environmental considerations.

Course Outcomes		Cognitive Level
At the end of this course, students will be able to:		
CO1:	Explain quantum effects and the behaviour of materials at the nanoscale.	Apply
CO2:	Identify and classify various nanomaterials and describe their synthesis and characterization.	Apply
CO3:	Analyze the operation of emerging nanoelectronic devices like SETs, CNT-FETs, and FinFETs.	Analyze
CO4:	Apply nanotechnology principles to evaluate device applications and limitations.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High = 3, Medium = 2, Low = 1

Text Book

T1. T. Pradeep, Nano: The Essentials – Understanding Nanoscience and Nanotechnology, Tata McGraw-Hill, 2007.

Reference Books

R1. M. Ratner and D. Ratner, Nanotechnology: A Gentle Introduction to the Next Big Idea, Pearson Education, 2003

R2. K. E. Drexler, Engines of Creation: The Coming Era of Nanotechnology, Anchor Books, 1986.

R3. G. Timp (Ed.), Nanotechnology, Springer, 1999.

R4. C. P. Poole and F. J. Owens, Introduction to Nanotechnology, Wiley, 2003.

Web References

1. https://nptel.ac.in/courses/115104124
2. https://nptel.ac.in/courses/117102058
3. https://ocw.mit.edu/courses/6-701-introduction-to-nanoelectronics-spring-2010/

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

VERTICAL I

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course code: 23EVE001		Course Title: Advanced MOSFET Modeling	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

This course introduces advanced MOS device electrostatics, nano MOSFET design, and scaling challenges in modern CMOS technology. It covers FinFETs, carbon nanotube FETs, molecular transistors, and emerging nanoelectronic devices.

Module I **22 Hours**

MOS Electrostatic: MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two-dimensional confinement, scattering.

Design Of Nano MOSFET: MOSFET scaling, short channel effects - channel engineering - source/drain engineering - Halo implants, Retrograde channel profile, Shallow source/drain extensions, high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multi-gate transistors – single gate – double gate – triple gate – surround gate, quantum effects, gate stack – gate patterning – threshold voltage and gate work function requirements.

Module II **23 Hours**

Designing With FinFETS: FinFET structure for VLSI circuits and systems, basic features - Large geometry FinFET device operation – drain current formulation – short channel effects on threshold voltage, subthreshold leakage currents, quantum mechanical effects, surface mobility, high field effects.

Nanotube FET Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs.

Transistors At The Molecular Scale : Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Illustrate the physics and 1D and 2D electrostatistics of MOS devices and it ultimate limits.	Apply
CO 2: Mitigate the short channel effects and design issues of transistors.	Apply
CO 3: Design and analysis of nano structure and nanoelectronic devices using FINFETs, Nanotube FETs.	Analyze
CO 4: Demonstrate the spin-dependant electron transport in magnetic devices.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	2
CO2	3	-	-	-	-	-	-	-	-	-	-	-	2	2
CO3	-	3	-	-	-	-	-	-	-	-	-	-	2	2
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	2

High-3; Medium-2;Low-1

Text Book(s):

T1. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006

T2. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008

Reference Book(s):

R1. Saha, Samar K. FinFET devices for VLSI circuits and systems. CRC Press, 2020.

R2. SadamichiMaekawa, —Concepts in Spin Electronicsǁ, Oxford University Press (2006).

Web References:

1. https://onlinecourses.nptel.ac.in/noc20_ee13/preview

Course Code: 23EVE002		Course Title: Compound Semiconductor Devices	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on the principles of semiconductor physics and material science to apply and analyze the performance of high-speed and high-power devices, including MESFETs, HEMTs, and HBTs, using advanced materials and hetero-junction structures.

Module I **22 Hours**

Performance Parameters: Transit time, junction capacitance, ON resistance, Breakdown voltage, mobility, doping, geometry, temperature effects

Compound Semiconductor Materials: Overview of III–V and IV–IV materials: GaAs, InP, GaN, AlGaAs, InGaAs, SiC. Material properties: mobility, velocity-field characteristics, doping, bandgap. Band diagrams, heterojunctions, bandgap engineering.

Device Interfaces and Contacts: Metal-Semiconductor contacts: Schottky diodes. Issues with native oxides in MOS structures. Interface traps and material processing basics

Module II **23 Hours**

MESFETs: Structure, pinch-off, threshold voltage, DC characteristics, short-channel and velocity overshoot effects, Comparison: GaAs, InP, GaN-based MESFETs

HEMTs / MODFETs: Heterojunction structure, 2DEG formation, AlGaAs/GaAs and InGaAs/InP systems, High-speed characteristics.

Heterojunction Bipolar Transistors (HBTs): Working principle, advantages over BJTs, GaAs/InP HBT structures, SiGe HBTs, Surface passivation and high-frequency response

Emerging Devices (Brief Overview):

Resonant tunneling diodes (RTD) and hot electron transistors (concept only)

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply physical principles to evaluate high-speed/high-power behaviour in compound semiconductor devices.	Apply
CO2: Compare different III–V materials for their suitability in specific device applications.	Analyze
CO3: Analyze MESFET and HEMT operation using device characteristics and structures.	Analyze
CO4: Apply heterojunction concepts to understand and interpret HBT performance.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	2
CO2	-	3	-	-	-	-	-	-	-	-	-	-	2	2
CO3	-	3	-	-	-	-	-	-	-	-	-	-	2	2
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	2

High-3; Medium-2;Low-1

Text Book(s):

T1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications, Wiley & Sons.

T2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons.

Reference Book(s):

R1. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,

R2. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0 12-691740- X.

Web References:

1.https://ocw.mit.edu/courses/6-772-compound-semiconductor-devices-spring-2003/

2.http://electroscience.ece.cornell.edu/files/compoundsemiconductordevicephysics_2009_incompletefigures.pdf

Course Code: 23EVE003		Course Title: Design of Analog Filters and Signal Conditioning Circuits	
Course Category: Major		Course level: Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on CMOS circuit design of various Analog Filter architectures. The required signal conditioning techniques in a Mixed signal IC environment are also dealt in this course.

Module I **22 Hours**

FILTER TOPOLOGIES: The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad. **INTEGRATOR REALIZATION**: Lowpass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators. **SWITCHED CAPACITOR FILTER REALIZATION**: Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

Module II **23 Hours**

SIGNAL CONDITIONING TECHNIQUES: Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

SIGNAL CONDITIONING CIRCUITS: Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the operational and design principles for all the important active analog filter configurations.	Apply
CO 2: Design and gain working knowledge of signal conditioning techniques and the necessary guide lines in a Mixed signal IC environment.	Apply
CO 3: Design switched capacitor circuits	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	-	3	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Ramson Pallas-Areny, John G. Webster “Sensors and Signal Conditioning” , A wiley Inter science Publication, John Wiley & Sons INC,2001.

T2. R.Jacob Baker, ”CMOS Mixed-Signal Circuit Design”, John Wiley & Sons, 2008.

Reference Book(s):

R1. Design with Operational Amplifiers and Analog Integrated Circuits, 3rd Edition; Sergio Franco; Tata Mcgraw Hill Education Pvt. Ltd.; 2002

R2. Schauman, Xiao and Van Valkenburg, “Design of Analog Filters”, Oxford University Press, 2009.

Web References:

1. https://archive.nptel.ac.in/courses/117/108/117108107/
2. https://archive.nptel.ac.in/courses/117/106/117106030/

Course Code: 23EVE004		Course Title: Signal Integrity for High-Speed Design	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on transmission line theory and signal integrity principles in high-speed digital design, including the analysis of wave propagation, reflections, cross-talk, non-ideal effects, and power delivery challenges, enabling the design and evaluation of reliable high-speed interconnects and clock distribution networks.

Module I **23 Hours**

SIGNAL PROPAGATION ON TRANSMISSION LINES: Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out,logic switching , input impedance into a transmission line section, reflection coefficient, skin- effect, dispersion.

MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK: Multi-conductor transmission-lines, coupling physics, per unit length parameters,Near and far- end cross talk,

Module II **23 Hours**

NON-IDEAL EFFECTS: Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current, Connectors.

POWER CONSIDERATIONS AND SYSTEM DESIGN: SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis**.**

CLOCK DISTRIBUTION AND CLOCK OSCILLATORS: Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, cancelling parasitic capacitance,

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Identify sources affecting the speed of digital circuits.	Apply
CO 2: Identify methods to improve the signal transmission characteristics	Apply
CO 3: Analyze non-ideal effects.	Analyze
CO 4: Analyze system power dissipation and clocking strategies.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	-	3	-	-	-	-	-	-	-	-	-	-	3	3
CO4	-	3	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1.H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, January 2003.

T2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice

Reference Book(s):

R1.S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, January 2014.

R2. Eric Bogatin, Signal Integrity – Simplified , Prentice Hall PTR, 3rd Edition, June 2018.

Web References:

1.https://www.udemy.com/course/signal-integrity-basics-to-advanced-simulations-esteempcb/?srsltid=AfmBOoq67WQyRrlQ4uQ7Vh7pMrhm_dAW4TviLC7W-HtmEe6ls1YveQII&couponCode=LEARNNOWPLANS

2. https://onlinecourses.nptel.ac.in/noc24_ee67/preview

Course Code: 23EVE005		Course Title: Electronic Packaging Techniques	
Course Category: Major		Course level: Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on the course aims to familiarize students with cutting-edge technologies in PCB design and fabrication, preparing them for advanced applications in modern electronic systems.

Module I **22 Hours**

Definition of electronic systems and history of semiconductors. Products and levels of packaging; packaging considerations for handheld devices. Printed Wiring Board (PWB): definition and basics. Semiconductor basics and process flow: wafer fabrication, inspection, testing, and packaging. Packaging evolution and chip connection methods: wire bonding, Tape Automated Bonding (TAB), and flip chip**.**

Semiconductor Packages

Overview of Single Chip Modules (SCM), common and advanced package types. Packaging materials and thermal mismatch issues. Multichip Modules (MCM) and their types; System-in-Package (SiP); packaging roadmaps and hybrid circuits. Electrical design aspects: parasitics (R, L, C), layout considerations, reflection issues, and interconnects.

Module II **23 Hours**

CAD for PWBs:

Benefits of CAD in PCB design. Basics of DFM (Design for Manufacturability), DFR (Design for Reliability), and DFT (Design for Testability). Components of a CAD tool; schematic design, component layout, design rules, and DFM checks. Overview of CAD output files for fabrication.

PWB Technologies:

Board-level packaging concepts. PWB fabrication process: photo plotting, mask generation, vias, substrates, surface prep, photoresist, UV exposure, developing, etching, resist stripping, and screen printing. Through-hole and pattern plating methods. Solder mask and multilayer PWB introduction. Microvias and sequential buildup for HDI boards.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Explain the evolution of semiconductor packaging and the different levels and types of packaging used in electronic systems.	Apply
CO2: Illustrate the process flow of wafer fabrication, inspection, and packaging techniques including wire bonding, TAB, and flip chip technologies.	Apply
CO3: Apply design rules and CAD tools for schematic capture, component layout, and PCB design considering DFM, DFR, and DFT principles.	Apply
CO4: Analyze surface mount soldering processes, materials, and thermal management strategies for reliable electronic system packaging.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	-	3	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Rao R. Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001.

T2. S.A. Srinivasa Moorthy ,“Introduction to Electronic Packaging”, Notion press

Reference Book(s):

R1. William D. Brown, “Advanced Electronic Packaging”, IEEE Press, 1999.

R2. F. Patrick McCluskey , ” Electronic Packaging: Materials and Their Properties”, CRC Press Inc

Web References:

1. https://onlinecourses.nptel.ac.in/noc22_me61/preview
2. https://archive.nptel.ac.in/courses/112/105/112105267/

Course code: 23EVE006		Course Title: Network On Chip	
Course Category: Major		**Course level : Higher / Advanced**	
L:T:P(Hours/Week) 3: 0: 0	**Credits:3**	**Total Contact Hours:45**	**Max Marks:100**

Course Objectives:

To Understand the concept of Network on Chip, learn router architecture designs and to Study fault tolerance Network on Chip

Module I **22 Hours**

Introduction to NoC – OSI layer rules in NoC – Interconnection Networks in Network-on-Chip - Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support
Switching Techniques and Packet Format – Asynchronous FIFO Design - GALS Style of Communication – Wormhole Router Architecture Design - VC Router Architecture Design – Adaptive Router Architecture Design.

Packet routing-QoS, congestion control and flow control – router design – network link design – Efficient and Deadlock Free Tree-Based Multicast Routing Methods.

Module II **23 Hours**

Path-Based Multicast Routing for 2D and 3D Mesh Networks Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Demonstrate the use of NoC topologies, switching methods, and flow control protocols to develop efficient interconnection strategies.	Apply
CO2: Examine the design considerations of wormhole, virtual channel, and adaptive router architectures, including FIFO and GALS-based communication.	Analyze
CO3: Implement fault-tolerant and path-based multicast routing algorithms in 2D and 3D mesh-based NoC system	Apply
CO4: Investigate verification techniques, test strategies, and security mechanisms used in the design of robust NoC infrastructures.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Chrysostomos Nicopoulos, Vijay Krishnan Narayanan, Chita R. Das" Networks-on - Chip

"Architectures Holistic Design Exploration", Springer, 2010.

Reference Book(s):

R1. Fayez Gebali, Haytham El Miligi, Hqhahed Watheq E1-Kharashi, "Networks-on-Chips theory and practice" CRC press, 2009

R2. Konstantinos Tatas and Kostas Siozios "Designing 2 D and 3D Network-on-Chip Architectures" 2013.

R3. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014.

R4. Santanu Kundu, Santanu Chattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration", CRC Press, 2014Santanu Kundu, Santanu

Web References:

1. https://archive.nptel.ac.in/noc/courses/noc19/SEM1/noc19-cs02/
2. https://www.coursera.org/learn/comparch

VERTICAL II

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course code: 23EVE007		Course Title: Art of Analog Layout	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course aims to apply schematic fundamentals, CMOS process knowledge, and layout design flows for custom IC design. It focuses on implementing analog and advanced layout techniques to meet performance, electrical, and manufacturability requirements.

Module I **22 Hours**

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

Analog Layout Design: Isolation Techniques, STI, LOD, WPE, Matching Techniques, Parasitic Capacitance and Resistance.

Advanced Analog Layout Concepts: DFM – EMIR, Supply/Ground bounce, Self-Heating & Metal Density Effects, Decap, ERC, Antenna, Electrostatic Discharge.

Module II **23 Hours**

Advanced techniques for specialized building blocks: Standard cell libraries, Pad cells and Laser fuse cells, advanced techniques for building blocks, Power grid Clock signals and Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

Layout considerations due to process constraints: Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring , Minimizing Stress effects.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply design flows and fabrication basics to create custom CMOS circuits.	Apply
CO 2: Apply layout methods to improve analog circuit performance, robustness, and manufacturability.	Apply
CO3: Apply specialized layout techniques to meet high-performance, timing, and electrical reliability requirements	Apply
CO4: Apply layout methods to meet fabrication limits and ensure stable pad and device structures	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Alan Hastings, “The Art of Analog Layout” Pearson College Div, 6 July 2005.

T2. Helmut E. Graeb, “Analog Layout Synthesis: A Survey of Topological Approaches”, Springer-Verlag, October 2014

Reference Book(s):

R1. Koen Lampaert , Georges Gielen , Willy M.C. Sansen, “Analog Layout Generation for Performance and Manufacturability: 501”, Springer-Verlag , December 2010

R2. BapirajuVinnakota, “Analog and mixed-signal test”, Prentice Hall, 1998.

Web References:

1. https://archive.nptel.ac.in/courses/117/101/117101105/

Course Code: 23EVE008		Course Title: Mixed Signal Circuit Design	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to apply testing principles and measurement techniques for analog and mixed-signal circuits, including DACs, ADCs, and high-speed communication channels, with emphasis on yield analysis, test accuracy, and the use of automated test equipment in production environments.

Module I **22 Hours**

MIXED – SIGNAL TESTING: Common Types of Analog and Mixed- Signal Circuits – Applications of Mixed-Signal Circuits – Post Silicon Production Flow - Test and Packing – Characterization versus Production Testing - Test and Diagnostic Equipment - Automated Test Equipments – Wafer Probers – Handlers – E-Beam Probers – Focused Ion Beam Equipments – Forced –Temperature.

YIELD, MEASUREMENT ACCURACY, AND TEST TIME: Yield - Measurement Terminology - Repeatability, Bias, and Accuracy - Calibrations and Checkers - Tester Specifications - Reducing Measurement Error with Greater Measurement Time – Guardbands - Effects of Measurement Variability on Test Yield - Effects of Reproducibilty and Process Variation on Yield - Statistical Process Control.

Module II **23 Hours**

ADC TESTING: ADC Testing Versus DAC Testing - ADC Code Edge Measurements - Edge Code Testing Versus Center Code Testing, Step Search and Binary Search Methods, Servo Method, Linear Ramp Histogram Method, Histograms to Code Edge Transfer Curves, Rising Ramps Versus Falling Ramps, Sinusoidal Histogram Method - DC Tests and Transfer Curve Tests - Dynamic ADC Tests - Tests for Common ADC Applications.

CLOCK AND SERIAL DATA COMMUNICATIONS CHANNEL MEASUREMENT: Synchronous and Asynchronous Communications - Time-Domain Attributes of a Clock Signal - Frequency Domain Attributes of a Clock Signal - Communicating Serially Over a Channel - Bit Error Rate Measurement - Methods to Speed Up BER Tests in Production - Deterministic Jitter Decomposition - Jitter Transmission Tests.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply mixed-signal circuit fundamentals and their role in electronic systems.	Apply
CO2: Utilize key measurement terminologies to interpret and assess test results in mixed-signal testing environments.	Apply
CO3: Implement concepts of analog-to-digital conversion to evaluate ADC architectures and applications.	Apply
CO4: Perform ADC testing and examine clock signal attributes relevant to high-speed serial data communication systems.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Gordon W.Roberts, Friedrich Taenzler, Mark Burns, “An Introduction to Mixed-signal IC Test and Measurement” Oxford University Press, Inc.2012

T2. R. Jacob Baker, “CMOS: Mixed-Signal Circuit Design“, Wiley, 1 January 2008.

Reference Book(s):

R1.M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.

R2. BapirajuVinnakota, “Analog and mixed-signal test”, Prentice Hall, 1998.

Web References:

1. https://web.iitd.ac.in/~shouri/eel786/

Course Code: 23EVE009		Course Title: Data Converters	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to provide a clear understanding of MOS amplifier design, including DC biasing, small-signal models, and the gm/Id method. It also covers noise analysis in MOS circuits and explains stability and compensation techniques used in operational and feedback amplifiers.

Module I **22 Hours**

INTRODUCTION: Quantization noise, anti-aliasing filters, gain and offset errors, definitions of INL and DNL, SNR, SFDR, ENOB of ADC/DACs, finite duration pulse aperture effects, transistor matching, Bandgap reference design.

D/A CONVERTER DESIGN, SAMPLE AND HOLD CIRCUITS: Current Steering DACs, current cell design issues. Properties of MOS Switches, charge injection, bootstrapping, sampling jitter, thermal noise, Quantization noise and nonlinearity effects.

COMPARATOR DESIGN: Comparator architectures, metastability and yield, Clock feed through effects, switched capacitor amplifiers and offset cancellation.

Module II **23 Hours**

ADC/DAC ARCHITECTURES: SAR, Flash, Pipeline and time interleaved ADC topologies and their CMOS realizations issues. Error correction procedures for ADCs.

FEEDBACK AND STABILITY: Delta sigma modulators, alternative modulator architectures, quantization and noise shaping, decimation filtering, implementation of Delta sigma modulators, delta sigma DACs.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Design a various building blocks used in mixed signal (A/D and D/A converters) CMOS IC Design.	Apply
CO 2: Design a hand calculation for the above important functional blocks and enables the student to carry out circuit simulations and layout design.	Apply
CO 3: Design a carrier in the broad field of electronics and communication.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Marcel Pelgrom, "Analog to Digital Conversion", Springer Verlag, 2nd Edition, 2013.

T2. Shanthi Pavan, Richard Schreier, Gabor C. Temes , “Understanding Delta Sigma Data Converters”, Willey –IEEE Press, 2nd Edition, 2017.

Reference Book(s):

R1. Franco Malobreti "Data Converters", Springer Verlag, 2007

R2. Behzad Razavi,” Analysis and Design of Data Converters“, Cambridge Univ Pr, 30 June 2025.

Web References:

1. https://nptel.ac.in/courses/117106034

Course Code: 23EVE010		Course Title: Power Management and Clock Distribution Circuits	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course imparts knowledge on designing reference circuits, low dropout regulators, and clock generation/recovery circuits, with a focus on high-speed digital systems and oscillator selection.

Module I **22 Hours**

VOLTAGE AND CURRENT REFERENCES: Current mirrors, self-biased current reference, startup circuits, VBE based current reference, VT based current reference, band gap reference , supply independent biasing, temperature independent biasing, PTAT current generation, constant Gm biasing.

LOW DROP OUT REGULATORS: Analog building blocks, negative feedback, performance metrics, AC design, stability, internal and external compensation, PSRR – internal and external compensation circuits.

OSCILLATOR FUNDAMENTALS: General considerations, ring oscillators, LC oscillators, Colpitts oscillator, jitter and phase noise in ring oscillators, impulse sensitivity function for LC & ring oscillators, phase noise in differential LC oscillators.

Module II **23 Hours**

CLOCK DISTRIBUTION CIRCUITS: PLL fundamental, PLL stability, noise performance, charge-pump PLL topology, CPPLL building blocks, jitter and phase noise performance, DLL fundamentals.

CLOCK AND DATA RECOVERY CIRCUITS: CDR architectures, transimpedance amplifiers and limiters, CMOS interface, linear half rate CMOS CDR circuits, wide capture range CDR circuits.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Design band gap reference circuits and low drop out regulator for a given specification. And understand specification related to supply and clock generation circuits of IC	Apply
CO 2: Choose oscillator topology and design meeting the requirement of clock generation circuits.	Apply
CO 3: Design clock generation circuits in the context of high speed I/Os, high speed broad band communication circuits and data conversion circuits.	Apply
CO 4: Design clock distribution circuits	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Gabriel.a. Rincon-Mora, "Voltage References from Diode to Precision Higher Order Band gap circuits", John Wiley & Sons Inc, 2002.

T2. Gabriel.a. Rincon-Mora, "Analog IC Design with Low-Dropout Regulators", Mcgraw-Hil Professional Pub, 2009.

Reference Book(s):

R1.R1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mcgraw Hill, 2001

R2. Floyd M. Gardner ,"Phase Lock Techniques" John Wiley& Sons, Inc 2005.

Web References:

1. https://onlinecourses.nptel.ac.in/noc23_ee13/preview

Course Code: 23EVE011		Course Title: Radio Frequency IC Design	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to impart knowledge on fundamental RF IC design concepts, including noise, distortion, low-noise amplifiers, nonlinear circuits, modulators, demodulators, oscillators, PLLs, and basic transmitter/receiver architectures, enabling them to apply and analyze essential RF circuit design principles in practical contexts.

Module I **22 Hours**

Introduction to RF IC Design Principles: Basic concepts of RF signals, frequency spectrum, and challenges in RF IC design. Overview of noise sources in RF circuits and their impact on system performance. Introduction to distortion and linearity in RF circuits. Understanding S-parameters and impedance matching techniques for RF ICs**.**

Wireless communication standards: WLAN, Bluetooth, LTE, 5G NR, and their frequency bands.

Low-Noise Amplifiers and Resonant Circuits: Principles of low-noise amplifier (LNA) design including noise figure, gain, and stability criteria. Design approaches for LNAs in CMOS technology. Basics of resonant circuits and their role in RF filtering and amplification. Impedance matching using inductors and capacitors in IC design.

Module II **23 Hours**

Nonlinear RF Circuits and Modulation Techniques: Characteristics of nonlinear RF devices and their effect on signal quality. Introduction to RF modulators and demodulators including AM, FM, and phase modulation schemes. Design considerations for mixers and frequency converters in RF ICs.

Oscillators, Phase-Locked Loops, and Transmitter/Receiver Architectures: Fundamentals of RF oscillators and phase noise. Overview of phase-locked loops (PLL) and frequency synthesis in RF ICs. Basic transmitter and receiver architectures including direct-conversion and superheterodyne receivers. Introduction to multiple access techniques such as FDMA, TDMA, and CDMA.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply fundamental RF IC design concepts, noise analysis, impedance matching, and wireless communication standards to real-world circuit scenarios.	Apply
CO 2: Analyze the design, performance, and implementation of low-noise amplifiers and resonant circuits in CMOS technology.	Analyze
CO3: Apply nonlinear circuit principles and modulation techniques for designing mixers and frequency converters in RF ICs.	Apply
CO4: Analyze oscillator, phase-locked loop functions, and basic transmitter/receiver architectures used in modern RF communication systems.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-	2	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO4	-	3	-	-	-	-	-	-	-	-	-	-	2	3

High-3; Medium-2;Low-1

Text Book(s):

T1. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd Edition, Cambridge University Press, 2004, ISBN-13: 978-0521835393, ISBN-10: 0521835393.

T2.B. Razavi, RF Microelectronics, 2nd Edition, Prentice Hall, 2011, ISBN-13: 978-0137134731, ISBN-10: 013713473X.

T3.P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd Edition, Oxford University Press, 2002, ISBN-13: 978-0195142704, ISBN-10: 0195142707.

Reference Book(s):

R1. D. M. Pozar, Microwave Engineering, 4th Edition, Wiley, 2011, ISBN-13: 978-0470631553, ISBN-10: 0470631554.

R2. K. Sam Shanmugam, RF and Microwave Circuit Design: Theory and Applications, Wiley, 2016, ISBN-13: 978-1119063749, ISBN-10: 111906374X.

Web References:

1. https://archive.nptel.ac.in/courses/117/102/117102012/

Course Code: 23EVE012		Course Title: PCB and System Design	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course is intended to apply basic concepts of PCB and system design using design software, address mechanical and manufacturing challenges, and implement modern techniques in PCB design and fabrication.

Module I **22 Hours**

Introduction to PCB Design:

Fundamentals of electronic components and circuits, PCB materials and types (single and multilayer), layout planning, ground, and thermal considerations.

PCB Design Workflow and EDA Tools:

Overview of EDA tools (EasyEDA, KiCad, Altium Designer), footprint selection, through-hole and SMD components, form factors, padstack design, PCB layout (manual and auto-routing), silkscreen legend, netlisting, and Gerber file generation.

Fabrication Process and Prototyping:

Fabrication of a simple circuit (e.g., 555 timer-based astable multivibrator), file formats for fabrication (bitmap, PNG, vector, Gerber), PCB etching, drilling, tinning, soldering (SMD and through-hole), and inspection techniques.

Module II **23 Hours**

Enclosure Design and Standards:

Enclosure fabrication using CO_2 laser and foam board cutting. Introduction to IC packaging, PCB recycling techniques, and key IPC and NEMA standards (IPC-A-600, IPC-2221, IPC-2581, etc.).

Emerging PCB Manufacturing Techniques:

Introduction to additive manufacturing (SL, FDM, 3DP), materials and applications in PCB prototyping. Overview of modern PCB printers: Voltera V-One, BotFactory SV2, and LPKF plotter.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply the fundamental principles of PCB and system design in accordance with industry standards.	Apply
CO2: Use PCB design software to create simple circuit layouts and navigate the basic design process.	Apply
CO3: Design plated through-holes, surface-mount lands, and general layout footprints for PCB implementations.	Apply
CO4: Design enclosures for PCBs and apply different fabrication methods to produce functional circuit boards.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	2
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	2
CO3	-	-	3	-	-	-	-	-	-	-	-	-	3	2
CO4	-	-	3	-	-	-	-	-	-	-	-	-	3	2

High-3; Medium-2;Low-1

Text Book(s):

T1. T1. Kraig Mitzner, “Complete PCB Design Using OrCad Capture and Layout”, Newness, 1st Edition, 2009.

T2. Simon Monk, “Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards”, McGraw-Hill Education TAB; 2nd Edition, 2017.

Reference Book(s):

R1. Douglas Brooks, “Signal Integrity Issues and Printed Circuit Board Design”, Prentice Hall PTR, 2003.

R2.Lee W. Ritchey , John Zasio, Kella J. Knack, “Right the First Time: a Practical Handbook on High Speed PCB and System Design”, Speeding Edge , 2003.

Web References:

1. https://onlinecourses.nptel.ac.in/noc24_ee127/preview

VERTICAL III

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course code: 23EVE013		Course Title: Scripting Language for VLSI	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

To provide a thorough understanding of semiconductor devices and their operation in analog circuit design and to develop analytical and design skills for building and evaluating electronic amplifiers using BJTs and MOSFETs.

Module I **22 Hours**

Linux Basics

Introduction to Linux, File System of Linux, General usage of Linux kernel and basic commands, Linux users and groups, Permissions for files, directories and users, searching files and directories, Zipping and unzipping concepts, Introduction to Networking in Linux, Network basics and tools, File transfer protocols, Network file system, Shell scripting, Job scheduling (cron, at), Remote access and automation with ssh and expect.

Perl Scripting

Introduction, working with simple values, Lists and Hashes, Loops and Decisions, Regular Expressions, File and Data operations, References and Subroutines, Modules and Packages, Running and Debugging scripts, Object-Oriented Perl, Text file parsing, Log file analysis, Report

Module II **23 Hours**

Python Scripting

Introduction, Python Environment, Data types and Expressions, Modules and Libraries, Control structures, Functions and Classes, File I/O, List and Dictionary operations, String processing, Regular expressions, Exception handling, Object-oriented scripting, Parsing netlists, SDC, and SDF files, Automating synthesis/P&R/STA reports, TCL wrapper generation, Batch job control for EDA tools, Regression suite automation.

Tool Interfacing and Automation in VLSI Design Flow

Scripting for EDA tool automation: Synopsys, Cadence, Mentor tools, Generating Makefiles and build systems, Automating simulation (ModelSim, VCS, NC-Sim), synthesis (Design Compiler, Genus), and P&R (Innovus, ICC2),Parsing and processing tool reports (timing, power, area), Testbench automation, waveform generation/processing, Code coverage and functional

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Interpret the characteristics and operation of diodes, BJTs, and MOSFETs using appropriate models.	Apply
CO2: Design biasing circuits for BJTs and MOSFETs to achieve desired operating points.	Apply
CO3: Analyze single-stage and multi-stage transistor amplifiers for voltage gain and impedance.	Analyze
CO4: Determine the frequency response of BJT and MOSFET amplifiers using small-signal equivalent models	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	-	3	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Ganesh Sanjiv Naik, Learning Linux Shell Scripting, Packt Publishing Ltd.

T2. Larry Wall, Tom Christiansen, and John Orwant, Programming Perl, O'Reilly Media

T3. Hans Petter Langtangen, A Primer on Scientific Programming with Python, Springer.

Reference Book(s):

R1. Guido van Rossum and Fred L. Drake Jr., An Introduction to Python, Network Theory Ltd.

R2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 7th ed., Boston, MA, USA: Pearson, 2014.

R3. M. H. Rashid, Microelectronic Circuits: Analysis and Design, 3rd ed., Boston, MA, USA: Cengage Learning, 2011

R4. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed., Hoboken, NJ, USA: Wiley, 2009.

Web References:

1. https://nptel.ac.in/courses/106/106/106106145
2. https://www.tutorialspoint.com/unix/shell_scripting.htm
3. https://perldoc.perl.org/
4. https://docs.xilinx.com/r/en-US/ug835-vivado-tcl-commands
5. https://nptel.ac.in/courses/106/106/106106212

Course Code: 23EVE014		Course Title: Algorithms for VLSI	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

ThE course introduces VLSI design methodologies, emphasizing physical design steps and modern automation tools. It focuses on algorithmic techniques for partitioning, placement, routing, and synthesis.

Module I **22 Hours**

INTRODUCTION: Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools. **DATA STRUCTURES AND BASIC ALGORITHMS:** Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

Module II **23 Hours**

ALGORITHMS FOR PARTITIONING AND PLACEMENT: Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithm. **ALGORITHMS FOR FLOORPLANNING AND ROUTING:** Floor planning – Problem Formulation – Floor planning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing. **MODELLING, SIMULATION AND SYNTHESIS:** Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply VLSI design flows and tools to implement modern physical design processes and design styles.	Apply
CO 2: Apply data structures and algorithms for graph-based optimization in VLSI design.	Apply
CO 3 :. Apply algorithmic techniques for layout compaction, partitioning, placement, floor planning, and routing in VLSI design.	Apply
CO4 :. Analyze modeling, simulation, and synthesis techniques to evaluate the functional correctness and design efficiency of VLSI systems.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	-	3	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India 2017.

T2. Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition,

Reference Book(s):

R1. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2008

R2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer, October 2012.

Web References:

1. https://archive.nptel.ac.in/courses/106/105/106105161/

Course Code: 23EVE015		Course Title: Physical Design and Automation	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course aims to cover physical design automation and emerging trends in VLSI design cycles, apply layout compaction and standard cell optimization, perform simulation and synthesis from gate to high-level abstraction, and implement advanced synthesis techniques for efficient hardware realization.

Module I **22 Hours**

VLSI Physical Design Automation: VLSI design cycle, new trends in VLSI design cycle, Physical design cycle, Design styles, System packing styles- Die packing and attachment styles.

Layout compaction: Standard cell layout, Layout compaction, Design rules, symbolic layout, problem formulation, Algorithms for constraint-graph compaction.

Module II **23 Hours**

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, Implementation, construction, and manipulation. Two level logic synthesis. High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment, and scheduling.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply VLSI design and physical design cycles, design styles, and die packing techniques.	Apply
CO 2: Apply layout compaction methods to optimize cell layouts while ensuring rule compliance and efficient placement	Apply
CO 3 : Apply modeling, simulation, and logic optimization techniques for efficient digital circuit design.	Apply
CO4 : Apply methods to convert high-level algorithms into optimized hardware structures with efficient resource usage and timing.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	2	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	3

High-3; Medium-2;Low-1

Text Book(s):

T1. S. H. Gerez, Algorithms for VLSI Design Automation , WILEY student edition, John wiley & Sons (Asia) Pvt. Ltd. 1999.

T2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation , Springer International Edition 3 rd edition, 2005

Reference Book(s):

R1. Hill &Peterson, Computer Aided Logical Design with Emphasis on VLSI , John Wiley, 1993.

R2. Wayne Wolf, Modern VLSI Design: Systems on silicon , Pearson Education Asia, 2 nd Edition,1998.

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview

Course Code: 23EVE016		Course Title: Reconfigurable Computing System and Applications	
Course Category: Major		Course level: Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course introduces reconfigurable computing systems and their architectural features, emphasizing FPGA design using Verilog, C, and Simulink. It focuses on design mapping, optimization, and hardware/software partitioning. Students will gain practical skills through real-world FPGA applications like image compression and network processing.

Module I **22 Hours**

Reconfigurable Computing System and Architectures: Introduction to Reconfigurable Computing Systems Evolution and Characteristics of Reconfigurable Systems Advantages and Challenges in Reconfigurable Computing. **Programming Reconfigurable Computing Systems:** Compute Models and System Architectures FPGA Programming with Verilog HDL Compiling C for FPGA Streaming FPGA Applications using Simulink Block Diagrams Operating System Support for Reconfigurable Computing. **Designs Mapping For Reconfigurable Platforms:** Technology Mapping-FPGA Design Optimization Strategies-Data path Composition Circuit Layout Specification on FPGAs-Path Finder: Performance-driven FPGA Routing-Retiming and Re-pipelining Techniques-Configuration Bit-stream Generation-Fast Compilation Techniques.

Module II **23 Hours**

FPGA Application Development: Implementing Applications with FPGAs-Precision Analysis for Fixed-point Computation-Distributed Arithmetic-CORDIC Architectures for FPGA Computing-Hardware/Software Partitioning. **Case Studies of FPGA Applications**: SPIHT Image Compression-Automatic Target Recognition Systems-Multi-FPGA Systems: Logic Emulation-Floating Point Considerations-Network Packet Processing-Memory-centric Computation (Active Pages).

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the fundamentals of reconfigurable computing and reconfigurable architectures.	Apply
CO 2: Apply knowledge of FPGA architectures to address design challenges in reconfigurable computing systems.	Apply
CO 3 : Apply FPGA design techniques such as fixed-point precision analysis, distributed arithmetic, and CORDIC architectures to implement efficient hardware/software partitioned applications.	Apply
CO4 : Apply FPGA-based design approaches to implement and analyze real-time applications such as image compression, target recognition, logic emulation, and network packet processing.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	2
CO2	3	-	-	-	-	-	-	-	-	-	-	-	2	2
CO3	3	-	-	-	-	-	-	-	-	-	-	-	2	2
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	2

High-3; Medium-2;Low-1

Text Book(s):

T1. Scott Hauck and Andre` DeHon, “Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation,” Morgan Kaufmann, July 2010.

T2. Stephen M. Trimberger, “Field – programmable Gate Array Technology”, Springer, 2007.

Reference Book(s):

R1. Clive Maxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools and Flows”, Newnes, Elsevier, 2006.

R2. Christophe Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications Paperback, Softcover reprint of hardcover 1st ed. 2007October, 2010

Course code: 23EVE017		Course Title: Machine Learning in VLSI Design	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course aims to introduce machine learning architectures and their hardware implementation using VLSI techniques. It focuses on designing and optimizing neural network models, including deep learning architectures, for efficient hardware realization.

Module I **22 Hours**

Introduction to Machine Learning Architecture: Artificial Neural Networks – Artificial Neuron and its mathematical model - Neural network architecture: single layer and multilayer feed forward networks, Learning Paradigms Supervised, Unsupervised and reinforcement Learning, Architecture for Multiply and Accumulate unit, Special function unit for Sigmoid and ReLu activation functions.

Supervised Learning and Unsupervised Learning: Multilayer Perceptron - Back propagation learning algorithm, 9 Radial-basis function Networks Kernels and Support vector machines, Unsupervised learning - K Nearest Neighbors , Self-organizing Feature Maps.

Module II **23 Hours**

VLSI Implementation of Neural Networks: Processing element model, PE row, PE array design - Processing element tile design - Direct, FFT-based, Winograd-based, Matrix multiplication based convolutional strategies.

Deep Neural Networks: Convolutional Neural basics: kernels, padding, stride, channels, activation maps - Standard CNN architectures: LeNet, AlexNet, VGG, Inception, ResNet, GoogleNet, DenseNet; Performance comparison of different CNN architectures.

VLSI Architecture for Deep Neural Networks: VLSI architecture for deep neutral networks, data and instruction flow in 2D systolic array architecture - Processing optimization in 2D systolic array - Hardware Accelerator.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply neural network architectures and learning paradigms to design and implement MAC units and activation function blocks for machine learning models.	Apply
CO2: Apply machine learning algorithms on hardware platforms for real-time inference tasks.	Apply
CO3: Apply VLSI design techniques to implement neural network processing elements and convolutional strategies, and evaluate the performance of standard CNN architectures for hardware realization.	Apply
CO4: Apply VLSI architectural concepts to design and optimize 2D systolic arrays and hardware accelerators for deep neural network processing.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	2	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verlag.

T2. Jose G. Delgado-Frias, William R. Moore, “VLSI For Artificial Intelligence And Neural Networks,” Springer Science Business Media, LLC, 2001.

T3. Mohamed I. Elmasry, “VLSI Artificial Neural Networks Engineering”, Springer Science Business

Reference Book(s):

R1. Sied Mehdi Fakhraie, Kenneth C. Smith, “VLSI - Compatible Implementations for Artificial Neural Networks”, Springer Science Business Media, LLC, 1996.

R2. Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019. VLS 5234: Physical D

Web References:

1. https://nptel.ac.in/courses/117106092

Course Code: 23EVE018		Course Title: Hardware Security and Cryptography	
Course Category: Major		Course level: Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course provides a foundational understanding of cryptography and network security, covering symmetric and public-key systems, hash functions, and digital signatures. It emphasizes key management, user authentication, and secure communication across network layers. Students will also explore firewalls, intrusion detection, and emerging security trends in blockchain, cloud, and IoT.

Module I **22 Hours**

Introduction: Basics of cryptography, conventional and public-key cryptography, hash functions, authentication, and digital signatures. **Key Management and Authentication:** Key Management and Distribution: Symmetric Key Distribution, Distribution of Public Keys, X.509 Certificates, Public-Key Infrastructure. User Authentication: Remote User-Authentication Principles, Remote User-Authentication Using Symmetric Encryption, Kerberos Systems, Remote User Authentication Using Asymmetric Encryption. **Access Control and Security:** Network Access Control: Network Access Control, Extensible Authentication Protocol, IEEE 802.1X Port-Based Network Access Control - IP Security - Internet Key Exchange (IKE). Transport-Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS standard, Secure Shell (SSH) application.

Module II **23 Hours**

Application Layer Security: Electronic Mail Security: Good Privacy, S/MIME, Domain Keys Identified Mail. Wireless Network Security: Mobile Device Security. **Security Practices:** Firewalls and Intrusion Detection Systems: Intrusion Detection Password Management, Firewall Characteristics Types of Firewalls, Firewall Basing, Firewall Location and Configurations. Blockchains, Cloud Security and IOT security

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply symmetric and asymmetric encryption techniques to secure communication systems.	Apply
CO 2: Apply access control mechanisms and secure communication protocols to implement and analyze network and transport-level security in real-world applications.	Apply
CO 3 : Apply application-layer security techniques to secure email communication and protect wireless networks and mobile devices.	Apply
CO4 :. Apply security practices by configuring firewalls, managing intrusion detection systems, and implementing security measures for blockchain, cloud, and IoT environments.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Cryptography and Network Security: Principles and Practice, 6th Edition, William Stallings, 2014, Pearson, ISBN 13:9780133354690.

T2. Fault Tolerant Architectures for Cryptography and Hardware Security (Compute Architecture and Design Methodologies) , Sikhar Patranabis, Debdeep Mukhopadhyay Springer Verlag, Singapore, 2018

Reference Book(s):

R1. Network Security: Private Communications in a Public World, M. Speciner, R. Perlman, C. Kaufman, Prentice Hall, 2002.

R2. Network Security, Firewalls and VPNs, J. Michael Stewart, Jones & Bartlett Learning, 2013, ISBN-10: 1284031675, ISBN-13: 978-1284031676.

R3. The Network Security Test Lab: A Step-By-Step Guide, Michael Gregg, Dreamtech Press, 2015, ISBN-10:8126558148, ISBN-13: 978-8126558148.

Web References:

1. https://nptel.ac.in/courses/106105162

Course Code: 23EVE019		Course Title: Introduction to VLSI Life Cycle	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course introduces various VLSI verification techniques and automation scripting. It also focuses on developing a reusable UVM test bench environment.

Module I **22 Hours**

VLSI Design Flow: System & Architectural Design: Defining a system specification, performance analysis, cost analysis, identifying various functional blocks/modules; categorizing them in terms of digital, analog, RF and mixed signal blocks. Verification and Testing: Functional verification, logic design: Verifying the functionality of blocks, behavioural description, logic minimization, synthesis, verification, and testing.

Module II **23 Hours**

Circuit Optimization and Physical Design: Optimization of synthesized blocks for various performance metric, Introduction to placement and route, Layout Vs Schematic (LVS) verification, Design for Manufacturability. **Tape Out:** Post layout simulations, Process Voltage Testing, Process Design Kit, Design Rule Check, GDSII. **Fabrication and Packaging:** Fabrication and Packaging: CMOS process flow, dicing, various types of packaging.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the principles of VLSI design flow to develop basic digital and analog circuit layouts.	Apply
CO 2: Apply testing methodologies such as scan chains and BIST to ensure circuit reliability and fault tolerance.	Apply
CO 3 : Apply circuit optimization, placement & routing, LVS checks, and DFM techniques in physical design.	Apply
CO4 : Apply post-layout checks, DRC, GDSII export, CMOS fabrication, dicing, and packaging for tape out.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Sneh Saurabh, “Introduction to VLSI Design flow”, Cambridge University Press.

T2. N. H. E. Weste and C. Harris, “Principles of CMOS VLSI Design: A System Perspective, 3rd Edition, Pearson Education 2007.

Reference Book(s):

R1. R1. M.Morris Mano and Michel.D.Ciletti, Digital Design with an introduction to HDL, VHDL and Verilog, Sixth edition Pearson education.

R2. Jhon puyemura, “Introduction to VLSI CIRCUITS AND SYSTEMS”, Shree Hari Publications, January 2021

Web References:

1. https://nptel.ac.in/courses/117106092

Course code: 23EVE020		Course Title: VLSI Technology	
Course Category: Major		Course level: Higher / Advanced	
L:T:P (Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course covers the fundamentals of semiconductor material properties, crystal growth, wafer cleaning, oxidation, lithography, diffusion, ion implantation, thin film deposition, etching techniques, and metallization processes involved in integrated circuit fabrication.

Module I **22 Hours**

Introduction and Oxidation: Electronic Materials: Crystal Structures, Defects in Crystals, Si, Poly Si, Si Crystal Growth. Clean room and Wafer Cleaning: Definition, Need of Clean Room, RCA cleaning of Si. Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants, Dopant Redistribution, Oxide Charges, Device Isolation, LOCOS, Oxidation System.

Lithography and Diffusion: Overview of Lithography, Radiation Sources, Masks, Photoresist, Components of Photoresist Optical Aligners, Resolution, Depth of Focus, Advanced Lithography: E-beam Lithography, X ray Lithography, Ion Beam Lithography. Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin's Curves, Diffusion System.

Module II **23 Hours**

ION Implantation: Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask, Energy Loss Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post Implantation Annealing, Ion Channeling, Multi Energy Implantation.

Thin Film Deposition: Physical Vapor Deposition: Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering Chemical Vapor Deposition: Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques, reaction types, Boundaries and Flow **Etching:** Anisotropy, Selectivity, Wet Etching, Plasma Etching, Reactive Ion Etching. Overview of Interconnects, Contacts, Metal gate/Poly Gate, Metallization, Problems in Aluminum Metal contacts, Al spike, Electro migration, Metal Silicide, Multi-Level Metallization, Planarization, Inter Metal Dielectric.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Build the CMOS process flow by organizing key fabrication steps in sequence.	Apply
CO 2: Identify and select appropriate techniques involved in major microfabrication processes.	Apply
CO 3:Utilize advanced IC fabrication methods for enhanced performance and efficiency.	Apply
CO 4: Develop insight into technology scaling and **solve** issues related to advanced CMOS process fabrication.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	2
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Silicon VLSI Technology, Plummer, Deal and Griffin ,1st Edition, Pearson Education,2009

T2. Fundamental of Semiconductor Fabrication, Sze and May,2nd Edition, Wiley India, 2009

Reference Book(s):

R1. Silicon Process Technology, S K Gandhi,2nd Edition, Wiley India,2009.

R2. Hwaiyu Geng**,** *Semiconductor Manufacturing Handbook*, 2nd Edition, McGraw-Hill (July 11, 2023).

Web References:

1. https://archive.nptel.ac.in/courses/108/101/108101089/
2. https://archive.nptel.ac.in/noc/courses/noc15/SEM1/noc15-ec02/

Course Code: 23EVE021		Course Title: Memory Devices and circuits	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The Course aims to provide a comprehensive understanding of memory hierarchy and architectures, covering SRAM, DRAM, Flash, and emerging non-volatile memory technologies. It focuses on memory cell design, operation, scaling challenges, reliability, and layout considerations, including advanced topics like FinFET-based SRAM, 3D NAND Flash, and compute-in-memory concepts.

Module I **22 Hours**

Introduction to Memory Hierarchy: Introduction to Memory to memory Array Architecture-Generic Memory array diagram, memory cell size equivalent bit area - Memory Arrays Area Efficiency-**SRAM -**6T SRAM Cell Operation, SRAM stability analysis, SRAM's Leakage, Variability and reliability, SRAM Layout and scaling FinFET-based SRAM. **DRAM:** DRAM Overview- 1T1C Cell operation DRAM Technology, DRAM scaling, 3D Stacked DRAM, Embedded DRAM.

Module II **23 Hours**

Flash Memory: Flash Overview, Flash device physics, Flash Array Architectures Multilevel Cell, Flash Reliability, Flash scaling challenges,3D NAND Flash. **Emerging Non-Volatile Memory:** Overview of ENVM, Phase change memory (PCM), Resistive random access memory (RRAM), Magnetic random access memory (MRAM), Ferroelectric memories, Compute- in-memory.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply memory hierarchy and array architecture concepts to analyze memory cell efficiency.	Apply
CO 2: Apply DRAM design principles and scaling techniques to implement and evaluate memory systems using 1T1C cells, 3D-stacked, and embedded DRAM technologies.	Apply
CO 3: Apply architectures including 3D NAND and multilevel cell design for high-density storage applications.	Apply
CO4 : Apply emerging non-volatile memory technologies for advanced VLSI memory design.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. S. Aritome, NAND Flash Memory Technologies, 1st ed., 2016, Wiley-IEEE Press, Hoboken, NJ, USA, ISBN: 978-1119132608.

T2. Betty Prince ,Semiconductor Memories , 2nd ed.,2000, John Wiley & Sons- IEEE Press

Reference Book(s):

R1. Shimeng Yu, Semiconductor Memory Devices and Circuits, 1st ed., April 15, 2022, by CRC Press

R2. Ashok K. Sharma**,** Advanced Semiconductor Memories*, 1st ed., October 14,*

Web References:

1. https://onlinecourses.nptel.ac.in/noc21_ee86/preview

Course Code: 23EVE022		Course Title: Low Power VLSI Design Techniques	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

To understand the fundamental sources and mechanisms of power dissipation in CMOS circuits and explore hierarchical low-power design techniques. The course aims to equip students with methods for power estimation and optimization at various design levels, including logic, circuit, architecture, and software.

Module I **22 Hours**

Power Dissipation in CMOS: Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in MOS devices – Basic principle of low power design. Power Optimization: Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of low power adders and multipliers. Design of Low Power Circuits: Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock.

Module II **23 Hours**

Power Estimation: Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis Probabilistic power analysis. **Synthesis and Software Design For Low Power:** Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply techniques to estimate and minimize power dissipation in MOS circuits.	Apply
CO 2: Apply low-power design techniques to optimize combinational logic, sequential circuits, memory, and clock systems.	Apply
CO 3 : Apply power estimation techniques at various design abstraction levels to analyze and evaluate logic power consumption.	Apply
CO4 : Apply low-power synthesis techniques and software design strategies to optimize system performance and energy efficiency.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, January 2009.

T2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.

T3. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer October 2012.

Reference Book(s):

R1. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, October 2012.

R2. Abdelatif Belaouar, Mohamed.I. Elmasry, “Low power digital VLSI design”, Kluwer, September 2012.

R3. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons,inc. 2001.

Web References:

1. https://archive.nptel.ac.in/courses/106/105/106105034/

Course Code: 23EVE023		Course Title: SYSTEM ON-CHIP DESIGN	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The Course aims to provide a detailed understanding of System-on-Chip (SoC) architecture, design methodologies for logic, memory, and analog cores, as well as design validation and testing strategies. It emphasizes SoC design flow, integration challenges, simulation, verification, test techniques, and real-world case studies to develop reliable and reusable SoC solutions.

Module I **22 Hours**

Introduction: System tradeoffs and evolution of ASIC Technology-SoC Architecture-System on chip concepts and methodology – SoC design issues -SoC challenges and components. **System Design:** Design Methodological For Logic Cores- SoC Design Flow – On-chip buses –Design process for hard cores – Soft and firm cores – Core and SoC design examples. **System Memory:** Design Methodology for Memory and Analog Cores- Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase locked loops.

Module II **23 Hours**

Design Validation: Design Validation- Core level validation- Core validation plan –Test benches –SoC design validation – Protocol verification- gate level simulation –SoC Design Validation. **SoC Testing:** SoC Testing- SoC Test Issues –Cores without boundary scan – Cores with boundary scan -Test methodology for design reuse– Testing of microprocessor cores – Built in self-test method. **Case Study:** Validation and test of systems on chip.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply SoC design methodologies to develop basic system-on-chip architectures for embedded applications.	Apply
CO 2: Apply design methodologies for integrating embedded memories and analog cores such as ADCs and PLLs in system-on-chip architectures.	Apply
CO 3 : Apply validation and testing techniques to ensure functional correctness and reliability of SoC designs.	Apply
CO4 : Apply emerging techniques and technologies for the design of future SoC systems.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO2	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO3	3	-	-	-	-	-	-	-	-	-	-	-	3	3
CO4	3	-	-	-	-	-	-	-	-	-	-	-	3	3

High-3; Medium-2;Low-1

Text Book(s):

T1. Rochit Rajsunah,System-on-a-chip:DesignandTest,ArtechHouse,2007.

T2. PrakashRaslinkar, Peter Paterson &Leena Singh, System-on-a-chip verification

Reference Book(s):

R1. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System-on- Chip Design Series: Integrated Circuits and Systems, Springer,2007.

R2.L.Balado,E.Lupon,Validationandtestofsystemsonchip,IEEEconferenceonASIC/SOC,1999.

R3. A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line testing, 2000

Web References:

1. https://onlinecourses.nptel.ac.in/noc25_ee21/preview

Course code: 23EVE024		Course Title: Quantum Technology for Electronics Engineers	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

To introduce the fundamentals of quantum mechanics and their applications in electronic systems, with a focus on quantum devices, communication, sensing, and computing.

Module I **22 Hours**

Introduction to Quantum Mechanics for Engineering: Historical context and quantum vs classical technologies, Core postulates: wavefunctions, Dirac notation, Schrödinger equation (time-dependent & independent) **Mathematical Formalism & Qubit Representation:** Operators, uncertainty principle, superposition, entanglement, Qubits and quantum circuits: state vectors, density operators

Quantum Hardware Platforms: Physical implementations: superconducting qubits, trapped ions, photonic systems, Solid-state devices: quantum dots, silicon qubits, quantum tunneling effects. **Engineering Challenges & Decoherence:** Noise, decoherence

Module II **23 Hours**

Quantum Communication & Sensors: Quantum key distribution, entanglement, teleportation, Quantum sensors: atomic clocks, SQUIDs, gravitational-wave interferometry, Applied devices: quantum tunneling composites and sensing electronics. **Quantum Computing Basics:** Quantum gates, circuit design, universal gates, simple algorithms

Quantum Photonics & Nanocircuitry: Integrated quantum photonics: PICs, waveguides for qubits, Nano-scale circuits: quantum-dominated device behaviour in transistors, resonant tunneling diodes. **Industrial Outlook & Future Trends:** Emerging platforms, quantum-enabled electronics, commercialization challenges Ethical, security, societal implications of quantum tech

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply quantum mechanical principles to model qubits and interpret their behaviour in simple electronic systems.	Apply
CO2: Analyze the working principles and challenges of quantum hardware implementations like superconducting qubits and quantum dots.	Analyze
CO3: Apply the principles of quantum communication and sensing to evaluate their role in electronics and instrumentation.	Apply
CO4: Analyze quantum circuits and basic quantum algorithms to assess their computational and system-level impact.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	**3**	**-**	-	-	-	-	-	-	-	-	-	-	1	1
CO4	**-**	**3**	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Michael A. Nielsen and Isaac L. Chuang, Quantum Computation and Quantum Information Cambridge University Press.

Reference Book(s):

R1. David McMahon, Quantum Computing Explained, Wiley-IEEE Press.
R2. Chris Bernhardt, Quantum Computing for Everyone, MIT Press.
R3. Charles Kittel, Introduction to Solid State Physics, Wiley.
R4. Richard P. Feynman, Robert B. Leighton, and Matthew Sands, The Feynman Lectures on Physics, Vol. 3: Quantum Mechanics, Addison-Wesley.

Web References:

1. https://quantum-computing.ibm.com
2. https://azure.microsoft.com/en-us/products/quantum
3. https://brilliant.org/courses/quantum-computing
4. https://nptel.ac.in/courses/115/104/115104123

VERTICAL V

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course code: 23EVE025		Course Title: Embedded Systems	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course enables students to apply the fundamentals of embedded system design using RISC processors, software tools, Embedded C programming, real-time operating systems, and hardware/network interfaces to develop efficient and reliable embedded applications.

Module I **22 Hours**

Embedded Design Process and Hardware Components: Complex Systems and RISC processors - Embedded System Design Process - Formalism for System Design - CPU – CPU Bus–CPU performance-CPU Power Consumption – Memory System Mechanism– Configuring and Programming Input and Output Peripherals - Supervisor Mode, Exceptions and Traps - Coprocessors.

Software Tools and Embedded C Programming: Compilation process - Native Vs Cross-Compilers - Run-time libraries - Writing a library - Using Standard and alternative libraries – Partitioning methods – Kernels pop– Techniques for Emulation and Debugging – Embedded C Program Structure – Data types - Operators, expressions, and control statements – Functions and Procedures - Structures and union.

Module II **23 Hours**

Real Time operating System: Concurrent Software – Foreground/Background systems, Multi-threaded Programming, shared resources and Critical sections – Scheduling – Cyclic, Round-Robin, Priority based, Deadline driven and Rate Monotonic schedules – Memory Management – Shared Memory -Commercial operating systems. Evaluating operating system performance – Power optimization strategies for processes.

Hardware Accelerators & Networks: Multiprocessors- CPUs and Accelerators – Performance Analysis- Distributed Embedded Architecture – Networks for Embedded Systems: - I2C, UART, CAN Bus, Ethernet, Myrinet – Network based design – Internet enabled systems.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Identify the key hardware components and software tools used in embedded system development.	Apply
CO2: Develop real-time embedded applications using Embedded C programming methodology.	Apply
CO3: Utilize real-time operating system features to manage multitasking and system resources in embedded applications.	Apply
CO4: Integrate and select suitable communication protocols like I2C, UART, CAN, and Ethernet for embedded system development.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	1
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	2
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Wayne Wolf, "Computers as Components –Principles of Embedded Computing System Design", Morgan Kaufmann Publishers, 2nd Edition, June2008.

T2. Tammy Noergaard, “Embedded Systems Architecture”, Elsevier, 2006.

Reference Book(s):

R1. K.V.K.K.Prasad, “Embedded Real-Time Systems: Concepts, Design & Programming”, Dream tech press, 2005

R2. SteveHeath, "Embedded Systems Design", Newnes Publications, 2nd Edition,2003.

Web References:

1. .https://nptel.ac.in/courses/117105082

Course code: 23EVE026		Course Title: IOT Processors	
Course Category: Major		Course level: Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course aims to provide a comprehensive understanding of the ARM architecture, covering its core features, exception handling, and interrupt mechanisms in the CORTEX-M3 processor, along with an introduction to the architecture and capabilities of the STM32L15XXX series of ARM CORTEX-M3/M4 microcontrollers

Module I **22 Hours**

Overview Of Arm and Cortex-M3: ARM Architecture – Versions, Instruction Set Development, Thumb 2 and Instruction Set Architecture, Cortex M3 Basics: Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence, CORTEX M3 Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions, CORTEX M3 – Implementation Overview: Pipeline, Block Diagram. Bus Interfaces, I – Code Bus, D – Code Bus, System Bus-External PPB and DAP Bus. **Cortex Exception Handling and Interrupts:** Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor Call and Pendable Service Call, NVIC: Nested Vector Interrupt Controller, Overview, Basic Interrupts, SYSTICK Time, Interrupt Behaviour, Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail – Chaining Interrupts, Late Arrivals, and Interrupt Latency

Module II **23 Hours**

Cortex M3/M4 Programming: Overview, Typical Development Flow, Using C, CMSIS Using Assembly, Exception Programming Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation, Memory Protection Unit and other CORTEX M3 Features, MPU Registers, Setting up the MPU, Power Management, Multiprocessor Configuration.

STM32L15XXX ARM CORTEX M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control, STM32L15XXX Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART Development and Debugging Tools: Software and Hardware tools like Cross Assembler Compiler, Debugger, Simulator, In – Circuit Emulator (ICE), Logic Analyzer.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Identify the components of control systems and their suitable representations.	Apply
CO2: Solve time-domain parameters to determine the steady-state and transient response of systems.	Apply
CO3: Select appropriate frequency response methods to evaluate system performance.	Analyze
CO4: Develop state-space models and corresponding transfer functions for physical systems.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	-

Text Book(s):

T1. Joseph Yiu, The Definitive Guide to the ARM CORTEX M3/M4, Second Edition, Elsevier, 2010.

T2. Andrew N Sloss, Dominic Symes, Chris Wright, ARM System Developers Guide Designing and Optimising System Software, Elsevier, 2006.

T3. Michael J Flynn and Wayne Luk, Computer System Design, System On Chip, Wiley India 2011.

Reference Book(s):

R1 . Daniel W. Lewis, Fundamentals of Embedded Software with the ARM Cortex-M3, Pearson, 2012.

R2. Alexander G. Dean, Embedded Systems Fundamentals with ARM Cortex-M Based Microcontrollers: A Practical Approach, 2nd Edition, ARM Education Media, 2017.

Web References:

1. https://archive.nptel.ac.in/courses/117/106/117106111/

Course code: 23EVE027		Course Title: Embedded System Design with FPGA	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course imparts practical skills in embedded system design using FPGAs, covering digital platforms, embedded processors, hardware-software co-design, communication protocols, signal interfacing, motor control, and real-time prototyping.

Module I **22 Hours**

Introduction : Introduction to Embedded System Overview, Hypothetical Robot Control System, Digital Design Platforms - Microprocessor-based Design, Single-chip Computer/Microcontroller-based Design, Application Specific Standard Products (ASSPs), Design Using FPGA; **FPGA Devices** : FPGA and CPLD, Architecture of a FPGA - FPGA Interconnect Technology, Logic Cell, FPGA Memory, Clock Distribution and Scaling, I/O Standards, Multipliers, Floor Plan and Routing, Timing Model for a FPGA, FPGA Power Usage. **FPGA-based Embedded Processor**: Hardware Software Task Partitioning, FPGA Fabric Immersed Processors, Soft Processors, Hard Processors, Tool Flow for Hardware Software Co-design, Interfacing Memory to the Processor, Interfacing Processor with Peripherals, Types of On-chip Interfaces, Wishbone Interface, Avalon Switch Matrix, OPB Bus Interface, Design Re-use Using On-chip Bus Interface, Creating a Customized Microcontroller, Robot Axis Position Control.

Module II **23 Hours**

FPGA-Based Signal Interfacing And Conditioning: Serial Data Communication, Physical Layer for Serial Communication, RS-232-based Point-to-Point Communication, RS-485-based Multipoint Communication, Serial Peripheral Interface (SPI), Signal Conditioning with FPGAs. **Motor Control Using FPGA**: Introduction to Motor Drives, Digital Block Diagram for Robot Axis Control, Position Loop, Speed Loop, Power Module, Case Studies for Motor Control - Stepper Motor Controller, Permanent Magnet DC Motor, Brushless DC Motor, Permanent Magnet Rotor (PMR) Synchronous Motor, Permanent Magnet Synchronous Motor (PMSM). **Prototyping Using FPGA:** Prototyping Using FPGAs, Test Environment for the Robot Controller, FPGA Design Test Methodology, UART for Software Testing, FPGA Hardware Testing Methodology

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Design digital systems by utilizing FPGA architecture and embedded processors for real-time embedded applications.	Apply
CO2: Implement hardware-software co-design and serial communication interfaces using FPGA-based development tools.	Apply
CO3: Implement serial communication protocols and signal conditioning techniques using FPGA-based systems.	Apply
CO4: Design and test FPGA-based motor control systems and develop prototypes using appropriate hardware and software testing methodologies	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	1	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Rahul Dubay Introduction to Embedded System Design Using Field Programmable Gate Arrays, © 2009 Springer-Verlag London Limited

T2. Frank Vahid & Tony Givargis, Embedded System Design, A Unified Hardware/ Software Introduction, ISBN 978-0-471-38678-0 2014 .

Reference Book(s):

R1. Computers as Components, Principles of Embedded Computing System Design, by Wayne Wolf, Morgan Kauffman, 2022

R2. Alexander G. Dean, Embedded Systems Fundamentals with ARM Cortex-M Based Microcontrollers: A Practical Approach, 2nd Edition, ARM Education Media, 2017

Web References:

1. https://archive.nptel.ac.in/courses/117/108/117108040/
2. https://archive.nptel.ac.in/courses/108/105/108105186/

Course Code: 23EVE028		Course Title: Embedded Artificial Intelligence	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course enables students to understand the fundamentals of embedded systems and their constraints, and to explore AI techniques such as low-power, real-time optimized machine learning models suitable for embedded applications.

Module I **22 Hours**

Introduction To Embedded Ai : Definition and Importance of Embedded AI, Overview of Edge Computing in Embedded AI, Real-world applications of AI in embedded systems, AI at the Edge vs. Cloud Computing, Introduction to common embedded hardware platforms used for A applications, such as microcontrollers, system-on-chip (SoC) boards (e.g., Raspberry Pi, NVIDIA Jetson), Selection criteria for hardware platforms based on specific application requirements GPUs, TPUs, and other accelerators for inference tasks .

Importance of Machine Learning: Types of Machine Learning - Supervised, Unsupervised Reinforcement Learning; Machine Learning Workflow - Data pre-processing, Model Training Evaluation, Deployment; Machine Learning Algorithms for Embedded Systems – Regression Classification, Clustering, Dimensionality Reduction.

Module II **23 Hours**

Fundamentals of Deep Learning: Neural Networks: Structure and Functionality, Convolutiona Neural Networks (CNNs) for Image and Signal Processing, Recurrent Neural Networks (RNNs for Sequential Data, Training and Optimization – Back propagation and Gradient Descent, Hype parameter Tuning, Regularization Techniques.

Practical Considerations for Embedded AI: Embedded System Constraints - Memory, Powe Consumption, Size Constraints, Real-time Processing Requirements, Low Latency Inference Deployment of ML Models on Embedded Platforms - Frameworks and Tools for Deployment Optimization Techniques: Quantization, Pruning, Compression, Techniques for optimizing A algorithms for performance and power efficiency.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Identify the key components and constraints of embedded systems used in real-time applications.	Apply
CO2: Model AI-enabled embedded systems using optimized machine learning techniques for performance and energy efficiency.	Apply
CO3: Model AI-driven embedded systems by applying deep learning techniques tuned for performance and energy efficiency.	Apply
CO4: Develop embedded AI solutions using frameworks and tools that support model optimization for performance and power efficiency.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	2	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	2	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Joseph Yiu, The Definitive Guide to the ARM CORTEX M3/M4, Second Edition, Elsevier 2010.

T2. Andrew N Sloss, Dominic Symes, Chris Wright, ARM System Developers Guide Designing and Optimising System Software, Elsevier, 2006.

Reference Book(s):

R1 . Michael J Flynn and Wayne Luk, Computer System Design, System on Chip, Wiley India 2011.

R2. David Patterson & John L. Hennessy Computer Organization and Design: The Hardware/Software Interface (RISC-V Edition)**,** Morgan Kaufmann, 5th Edition, 2021.

Web References:

1. https://nptel.ac.in/courses/108105057

Course code: 23EVE029		Course Title: Data Analytics for IOT	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course enables students to learn the fundamental concepts of Big Data Analytics, gain exposure to IoT cloud analytics environments, understand IoT analytics techniques, examine the social impact of multimedia data, and identify real-world applications that integrate multimedia, Big Data, and IoT technologies.

Module I **22 Hours**

Introduction to Technological Developments: Defining IOT Analytics and Challenges- Defining IOT analytics, IOT analytics challenges, Business value concerns, IOT Devices and Networking Protocols- IOT devices, Networking basics, IOT networking connectivity protocols, analyzing data, IOT Analytics for the Cloud- Building elastic analytics, Designing for scale, Cloud security and analytics, The AWS, Microsoft Azure, The Thing Worx overview.

Cloud Analytics Environment: The AWS Cloud Formation, The AWS Virtual Private Cloud (VPC), terminate and clean up the Environment, data processing for analytics, big data technology to storage, Apache Spark for data processing, Handling change, Exploring and visualizing data, Techniques to understand data quality Techniques to understand data quality, R and RStudio.

Module II **23 Hours**

General Strategies on Extracting Value from Datasets: Decorating Your Data, communicating with Others Visualization and Dashboarding, Applying Geospatial Analytics to IOT Data, Data Science for IOT Analytics- Machine learning (ML), deep learning. **Societal Impact of Multimedia Big Data:** Multimedia Social Big Data Mining, Process Model, SWOT Analysis, Techniques for Social Big Data Analytics, Advertisement Prediction, MMBD Sharing on Data Analytics Platform, Legal/Regulatory Issues.

Application Environments: Big Data Computing for IOT Applications-Precision Agriculture, Machine Learning in Improving Learning Environment, Network-Based Applications of Multimedia Big Data Computing, Recent Trends in IOT-Based Analytics and Big Data, Future Directions and Challenges of Internet of Things.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Utilize Big Data and IoT concepts to explain and define cloud-based IoT analytics environments.	Apply
CO2: Select appropriate Big Data strategies based on the nature of data and application requirements	Apply
CO3: Evaluate the social impact of multimedia Big Data on privacy, communication, and digital behavior in modern society	Apply
CO4: Develop smart IoT solutions using Big Data frameworks for real-time analytics and automation.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	1
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	1

High-3; Medium-2;Low-1

Text Book(s):

T1. Andrew Minteer, “Analytics for the Internet of Things (IOT): Intelligent analytics for you intelligent devices”, Packt Publishing, first edition, July 2017.

T2. Sudeep Tanwar, Sudhanshu Tyagi, Neeraj Kumar, “Multimedia Big Data Computing fo IOT Applications: Concepts, Paradigms and Solutions”, Springer, 2020.

Reference Book(s):

R1. John Soldatos, “Building Blocks for IOT Analytics”, River Publishers Series In Signal, Image and Speech Processing, 2017.

R2. Nilanjan Dey, Aboul Ella Hassanien, Chintan Bhatt, Amira S. Ashour, Suresh Chandra Satapathy, “Internet of Things and Big Data Analytics Toward Next-Generation Intelligence”, Springer International Publishing, 2018.

Web References:

1. https://nptel.ac.in/courses/106105166
2. https://nptel.ac.in/courses/106106179

Course code: 23EVE030		Course Title: Privacy and Security in IOT	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objectives:

The course focuses on security threats, countermeasures, and privacy preservation in cyber-physical and IoT systems. It covers cryptographic techniques, secure system design, and threat mitigation in real-world applications.

Module I **22 Hours**

CYBER PHYSICAL SYSTEMS AND INTERCONNECTION OF THREATS: IoT and cyber-physicalsystems, IoT security (vulnerabilities, attacks, and countermeasures), security engineering for IoT development, IoT security lifecycle. Network Robustness of Internet of ThingsSybil Attack Detection in Vehicular Networks- Malware Propagation and Control in Internet of Things- Solution-Based Analysis of Attack Vectors on Smart Home Systems.

CRYPTO FOUNDATIONS: Block ciphers, message integrity, authenticated encryption, hash functions, Merkle trees, elliptic curves, public-key crypto (PKI), signature algorithms. **PRIVACY PRESERVATION FOR IOT:** Privacy Preservation Data Dissemination- Social Features for Location Privacy Enhancement in Internet of Vehicles- Lightweight and Robust Schemes for Privacy Protection in Key Personal IoT Applications

Module II **23 Hours**

TRUST MODELS FOR IOT: Authentication in IoT- Computational Security for the IoT- Privacy-Preserving Time Series Data Aggregation- Secure Path Generation Scheme for Real-Time Green Internet of Things- Security Protocols for IoT Access Networks- Framework for Privacy and Trust in IoT- Policy-Based Approach for Informed Consent in Internet of Things.

INTERNET OF THINGS SECURITY: Security and Impact of the Internet of Things (IoT) on Mobile Networks- Networking Function Security-IoT Networking Protocols, Secure IoT Lower Layers, Secure IoT Higher Layers, Secure Communication Links inIoTs, Back-end Security -Secure Resource Management, Secure IoT Databases, Security Products-Existing Test bed on Security and Privacy of IoTs, Commercialized Products.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply security techniques to identify and mitigate threats in IoT-based cyber-physical systems and networks.	Apply
CO2: Apply cryptographic methods and privacy-preserving techniques to secure data and enhance privacy in IoT applications	Apply
CO3: Apply trust models and security protocols to ensure authentication, privacy, and secure access in IoT networks and applications.	Apply
CO4: Apply IoT security protocols and mechanisms to ensure secure communication, data handling, and resource management across IoT networks and systems.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Hu, Fei. Security and privacy in Internet of things (IoTs): Models, Algorithms, and Implementations, 1stedition,CRC Press, 2016.

T2. Russell, Brian, and Drew Van Duren. Practical Internet of Things Security, 1 st edition Packt PublishingLtd, 2016.

Reference Book(s):

R1. Whitehouse O. Security of things: An implementers' guide to cyber-security for internet of things devices and beyond, 1 st edition, NCC Group, 2014

R2. DaCosta, Francis, and Byron Henderson. Rethinking the Internet of Things: a scalable approach toconnecting everything, 1 st edition, Springer Nature, 2013.

Web References:

1. https://onlinecourses.nptel.ac.in/noc23_cs13/preview

DIVERSIFIED

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course Code: 23ECE051		Course Title: Computer Architecture (Common to EA,EC,EV)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to impart knowledge on memory organization, addressing modes of a processor, the organization of cache memory and pipelining techniques for the design of high speed processor.

Module I **22 Hours**

Basic Structure of Computers:

Evolution of Microprocessor - Basic Processor Architecture - Operational concepts – Performance.

Instruction Set Architecture:

Memory location - Memory Operations – Instructions and sequencing - Addressing modes - CISC Vs RISC.

Basic Input/Output, Processing Unit :

Accessing I/O devices - Interrupts -Buses - Instruction Execution-DMA–Hardware Components – Instruction Fetch and Execution Steps – Control Signals-Hardwired Control - CISC Style Processors: Interconnect using Buses, Micro programmed Control.

Module II **23 Hours**

The Memory System: Characteristics of Memory Systems - Cache Memory Principles - Elements of Cache Design - Mapping Function - Example of Mapping Techniques - Replacement Algorithms - Performance Consideration.

Pipelining : Basic concept - Pipeline Organization and issues - Data Dependencies – Memory Delays – Branch Delays – Resource Limitations - Performance Evaluation - Superscalar operation –Pipelining in CISC Processors - Instruction Level Parallelism – Parallel Processing Challenges – Flynn’s Classification – Hardware multithreading – Multicore Processors: GPU, Multiprocessor Network Topologies.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the features of different instruction set architectures to evaluate their effect on system performance in real-world scenarios.	Apply
CO 2: Analyze various design elements to determine suitable memory organization for optimized performance.	Analyze
CO 3 : Examine the principles of pipelining and instruction-level parallelism to understand their impact on processor performance.	Analyze
CO 4: Independently learn about emerging computer architectures and deliver an oral presentation highlighting their impact on society and their contribution to sustainable and environmentally friendly technologies.(For Internal Assessment only)	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-		-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-	2	-
CO4	-	-	-	-	-	2	2	-	1	1	-	2	2	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Carl Hamacher, Zvonok Vranesic, Safwat Zaky, Naraig Manjikian, “Computer Organization and Embedded Systems”, 6th Edition, McGraw Hill, 2012

T2. David A. Patterson and John L. Hennessey, “Computer Organization and Design: The Hardware/Software Interface”, 5th Edition, Morgan Kauffman / Elsevier, 2014

Reference Book(s):

R1. William Stallings, “Computer Organization and Architecture: Designing for Performance”, 10th Edition, Pearson Education, 2016

R2. John L. Hennessey and David A. Patterson, “Computer Architecture: A Quantitative Approach”, Morgan Kauffman / Elsevier, 5th edition, 2012

Web References:

1. https://www.coursera.org/lecture/comparch/course-introduction-Ouq7L
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-823-computer-system-architecture-fall-2005/index.html
3. http://www.nptel.ac.in/courses/106102062/

Course Code: 23EEE014		Course Title: Industrial Automation (Common to EA,EC,EE,EV)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to cutting-edge technologies such as Programmable Logic Controllers (PLC), Supervisory Control and Data Acquisition (SCADA), and Distributed Control Systems (DCS), students will learn to develop innovative automation solutions. The course emphasizes hands-on experience in designing control logic programs, configuring industrial networks, and exploring real-world applications.

Module I **22 Hours**

Introduction to Factory Automation: History and developments in industrial automation- Vertical integration of industrial automation- Building blocks in Automation: Processing systems, Multi microprocessor systems, LAN, analog and digital I/O modules, remote terminal unit

Programmable Logic Controllers :PLC an Overview- Parts and Architecture of PLC- Principles of Operation - I /O Specifications - Memory types-Programming devices- PLC vs Computers, PLC size and Applications, Advantages of PLC, selection of PLC

Programming of PLC : Program scan - PLC Programming Languages-Simple process control programs using Relay Ladder Logic - Programming Timers : On delay timer, OFF delay timer- Programming counters: Up and Down counter – PLC arithmetic functions – Program Control Instructions-Math Instructions-data transfer operations-Data comparison instructions

Module II **23 Hours**

Industry Networking and SCADA :PLC Networking- Networking standards & IEEE Standard - Protocols - Field bus - Process bus and Ethernet .SCADA-Channel scanning-conversion to engineering units- data processing –Distributed SCADA systems- HMI introduction

Distributed Control System and Applications : DCS: Evolution – Different architectures – local control unit – Operator interface – Displays – Engineering interface. Applications: Thermal power plant-cement plant-water treatment plant- Solar, windmill substation automation.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply the principles of automation to identify its necessity in industrial processes.	Apply
CO 2: Analyze the architecture and types of PLCs used in industrial automation to select suitable options.	Analyze
CO 3 : Develop PLC-based control logic programs to meet specific industrial requirements.	Apply
CO 4: Analyze industrial networking protocols and SCADA systems to implement effective automation.	Analyze
CO 5: Apply the concepts of DCS to evaluate its applications in power plants and other industrial setups.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	3	-	-	-	-	-	-	-	3	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO5	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Frank D Petruzella “Programmable Logic Controllers", McGraw Hill Education India Private Limited, 6th Edition, 2023.

T2. Bolton.W, “Mechatronics”, Pearson Education, Delhi, 7th Edition,2018.

Reference Book(s):

R1. John W Webb & Ronald A Reis, “Programmable logic controllers: Principles and Applications”, Prentice Hall India, 5th edition, 2011

R2. Dobrivojie Popovic, Vijay P. Bhatkar,“ Distributed Computer Control for Industrial Automation”, Marcel Dekkar Inc., New York, 1st edition, 2011.

R3. Krishna Kant, „Computer based Industrial Control", Prentice Hall of India, 2nd edition, 2010

R4. Rajesh Mehra and Vikrant Vij, “PLCs& SCADA- Theory and Practice”, Laxmi Publications, 1st edition, 2019.

Web References:

1.http://www.fieldbus.org

2.www.nptel.ac.in/downloads/108105063/

3.http://nptel.ac.in/courses/108105062/18

Course Code: 23EEE085		Course Title: Automotive Electronics (Common to EA,EC,EE,EV)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The learners will be able to develop foundational knowledge of mechanical and electronic systems in modern automobiles. Additionally, the course focus on the role and implementation of embedded systems and X-by-wire technologies in automotive applications.

Module I **22 Hours**

Automotive Mechanical Systems: Overview of vehicle systems including the powertrain (air, fuel, ignition, exhaust and cooling), transmission types, braking systems, and steering mechanisms.

Electronics in Automotive Systems: Role of electronics in enhancing performance, control and compliance with legislation. Introduction to chassis subsystems (ABS, TCS, ESP), and comfort/safety features (airbags, seatbelt tensioners, cruise control).

Module II **23 Hours**

Drive-By-Wire Technologies: X-by-wire technologies: Steer-by-wire, brake-by-wire, shift-by-wire, and future trends.

Embedded Systems and EV Introduction: Sensor and actuator systems in gasoline/diesel engines (NOx, knock, MAP, oxygen, throttle position), thermal actuators, and body electronics (central locking, climate control). Introduction to electric vehicle classifications.

Vehicle Communication Protocols: Overview of SPI, I2C and automotive-specific protocols including CAN, LIN and MOST. Introduction to AUTOSAR framework for standardization and Ethernet.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Identify the key components and functions of automotive mechanical systems such as powertrain, transmission, braking, and steering, safety, and compliance.	Apply
CO2: Apply the role of electronic systems in enhancing vehicle performance, safety features, and regulatory compliance.	Apply
CO3: Examine the working principles of X-by-wire technologies and apply knowledge of sensors and actuators in automotive embedded system design.	Apply
CO4: Apply standard in-vehicle communication protocols to develop basic automotive communication systems and demonstrate the use of AUTOSAR for system integration.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO4	3	-	-	-	-	-	-	-	1	1	-	-	1	-

High-3; Medium-2;Low-1

Textbooks:

T1. Robert Bosch GmbH, "Bosch Automotive Handbook", 10th Edition, Wiley Publishers, 2019.

T2. William B. Ribbens, “Understanding Automotive Electronics”, 7th Edition, SAMS/Elsevier Publishing, 2012

Reference Book(s):

R1. Robert Bosch Gmbh, Automotive Electrics and Automotive Electronics, Systems and Components, Networking and Hybrid drive, 5th edition, Springer Vieweg, Wiesbaden 2014

R2. Knowles.D, Automotive Electronic and Computer Controlled Ignition Systems, Reston Pub Co,1990 R3. Denton.T , Automobile Electrical and Electronic Systems: Automotive Technology: Vehicle Maintenance and Repair, 2012

Web References:

1. www.austincc.edu/autotech
2. https://acconline.austincc.edu/webapps/portal/frameset.jsp

Course Code:23MEE008		Course Title: PLM for Engineers (Common to all Programmes)	
Course Category: Minor		Course Level: Higher	
L:T:P(Hours/Week) 2:0 : 2	Credits:3	Total Contact Hours: 60	Max Marks:100

Course Objectives:

The course is intended to apply Product Lifecycle Management (PLM) fundamentals and principles to develop strategies, manage product lifecycles, optimize engineering processes, configure Bills of Materials, and leverage digital manufacturing environments for practical applications and customer-centric use cases.

Module I **22 Hours**

Business Strategy in the PLM

Definition, PLM Lifecycle Model, Threads of PLM, Need for PLM, Opportunities and Benefits of PLM, Components and Phases of PLM, PLM feasibility Study, PLM Visioning, Strategy, Impact of strategy, implementing a PLM strategy, PLM Initiatives to Support Corporate Objectives, Infrastructure Assessment.

Business Processes in the PLM and Product Development Concepts

Characteristics of PLM, Environment Driving PLM, PLM Elements, Drivers of PLM, Conceptualization, Design, Development, Validation, Production, Support of PLM. Engineering Vaulting, Product Reuse, Smart Parts, Engineering Change Management, Workflow Management. Bill of Materials (E-BOM, M-BOM, S-BOM) and Process Consistency, Product Structure, Configuring BOM

Module II **23 Hours**

Digital Mock Up and Validation

Simulation Process Management, Variant Management, Digital Mock-Up and Prototype Development, Design for Environment, Virtual Testing and Validation, Marketing Collateral

Digital Manufacturing in the PLM

Digital Manufacturing, Benefits of Digital Manufacturing, Manufacturing the First-One, Ramp Up, Virtual Learning Curve, Manufacturing the Rest, Production Planning.

Customer Use Cases of the PLM

Impact and Challenges faced while implementing a successful PLM strategy -Rolls Royce, Nissan Motor, Sunseeker International , Xtrac ,kesslers international and monier and weatherford international.

List of Experiments: **15 Hours**

1. Demonstrate the 2-Tier & 4-Tier Architectures and Basic Team center applications like Organization, Project, and Schedule Manager.
2. Create CAD and Non-CAD datasets (MS Office, Notepad, etc.) by using explicit and implicit Check-In and Check-Out to create multiple iterations
3. Create the access control (Read, Write, and Delete) for the given dataset and block the access rights to other group members belongs to the same department. Also Perform the Impact Analysis (Where Used and Where Referenced) of a given dataset which is used in multiple assemblies.
4. Create the Product Structure in Structure Manager with 5 components assembled in first level and 3 components Assembled in second, third and fourth level with the sub-assemblies and export the assembly in local drive. Also, demonstrate the Variant Management.
5. Export the CAD dataset as a JT file and perform the various visualization tasks like Measurements, Sectioning, PMI, and Mark-up using JT2GO application

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO 1: Apply the fundamentals of PLM principles to develop a PLM strategy for a system.	Apply
CO 2: Apply PLM principles to manage product lifecycles, optimize engineering processes, and configure Bill of Materials with consistent workflows	Apply
CO 3 : Apply the Digital Manufacturing environment using PLM for use cases.	Apply
CO 4: Develop and present a report individually by applying various modules of PLM software for an engineering project.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	3	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	1	-	-	-
CO3	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO4	-	-	3	-	-	-	-	-	1	1	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. John Stark, “Product Lifecycle Management: Volume 1: 21st Century Paradigm for Product Realisation”, Springer International Publishing Switzerland, 4th edition, 2020.

T2. Grieves Michael, “Product Lifecycle Management- Driving the Next Generation of Lean Thinking”, McGraw-Hill, 2010.

T3. Wang, Lihui; Nee, Andrew Y.C. (Eds.) Collaborative Design and Planning for Digital Manufacturing, Springer, 2009.

Reference Book(s):

R1. Elangovan, U., “Product Lifecycle Management (PLM)”. Boca Raton, CRC Press, 2020.

R2. Fabio Giudice, Guido La Rosa, Product Design for the environment-A life cycle approach, Taylor & Francis 2006.

R3. Antti Saaksvuori, “ Product Life Cycle Management” - Anselmi Immonen, Springer, 3rd Edition, 2008.

Course Code:23MEE030		Course Title: Principles of Management (Common to EA,EC,EE,EV,ME)	
Course Category: Major		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

This course is intended to study the role of managers, the significance of planning, decision-making, and strategies in international business, the importance of organizing tasks, various motivational theories, and control techniques.

Module I **22 Hours**

OVERVIEW OF MANAGEMENT :

Organization – Management – Role of managers – Evolution of Management thought – Organization and the environmental factors – Managing globally – Strategies for International Business

PLANNING:

Nature and Purpose planning – Planning process – Types of Plans – Objectives – Managing by Objective (MBO) Strategies – Types of strategies – Policies – Decision Making – Types of decision – Decision Making Process – Rational Decision Making Process – Decision Making under different Conditions.

ORGANISING:

Nature and purpose of organizing – Organization structure – Formal and informal groups organization – Line and Staff authority – Departmentation – Span of Control – Centralization and Decentralization – Delegation of authority – Staffing – Selection and Recuritment – Orientation Career Development – Career stages – Training – Performance appraisal.

Module II **23 Hours**

DIRECTING :

Creativity and Innovation – Motivation and Satisfaction – Motivation Theories Leadership – Leadership theories – Communication – Hurdles to effective communication – organization culture – elements and types of culture – managing cultural diversity.

CONTROLLING:

Process of controlling – types of control – budgetary and non – budgetary control techniques – managing productivity – cost control – purchase control – maintenance control – quality control – planning operations.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO 1: Apply management principles to understand the roles and functions of managers in various organizational and business contexts.	Apply
CO 2: Develop and implement effective planning, decision-making, and strategic management practices to achieve organizational objectives in both domestic and international settings.	Apply
CO 3 : Prepare and present a seminar individually on organizational, motivational and control techniques including task allocation, employee engagement strategies, budgeting, and quality management to enhance productivity and efficiency.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	-	-	-	-	-	-	-	2	2	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. hen P. Robbins, Rolf Bergman and Mary Coulter, “Management”, Prentice Hall of India, 8th edition, 2017.

T2. Charles W.L Hill, Steven L McShane, “Principles of Management”, Mcgraw Hill Education, 2008

Reference Book(s):

R1. Hellriegel, Slocum & Jackson, “Management – A Competency Based Approach”, Thomson South Western, 10th edition, 2007.

R2. Harold Koontz, Heinz Weihrich and mark V Cannice, “Management – A global & Entrepreneurial Perspective”, Tata McGraw Hill, 12th edition, 2007.

R3. Andrew J. Dubrin, “Essentials of Management”, Thomson Southwestern, 7th edition, 2007

Course Code: 23SCE050		Course Title: Cyber security	
Course Category: Major		Course level : Higher / Advanced	
L:T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Pre-requisites

- Nil

Course Objectives: To provide foundational knowledge of cyberspace, cyber laws, and digital security practices to identify, prevent, and respond to cyber threats.

Module I **22 Hours**

Introduction to Cyber Security: Defining Cyberspace - Overview of Computer and Web-technology - Architecture of cyberspace, Internet, World wide web, Advent of internet, Internet infrastructure for data transfer and governance, Internet society, Regulation of cyberspace, Concept of cyber security, Issues and challenges of cyber security.

Cyber-crime and Cyber law: Classification of cyber-crimes - cyber-crime targeting computers and mobiles, cyber-crime against women and children, financial frauds, social engineering attacks, malware and ransomware attacks, zero day and zero click attacks, Cybercriminals modus-operandi , Reporting of cyber-crimes, Remedial and mitigation measures, Legal perspective of cyber-crime, IT Act 2000 and its amendments, Cyber-crime and offences, Organizations dealing with Cyber-crime and Cyber security in India, Case studies

Module II **23 Hours**

Social media and Security: Introduction to Social networks, Social media – Types, platforms, monitoring, Hashtag, Viral content, marketing, Challenges, opportunities and pitfalls in online social network, Security issues related to social media, Flagging and reporting of inappropriate content, Laws regarding posting of inappropriate content, Best practices for the use of Social media, Case studies.

E-Commerce and Digital Payments: E- Commerce - Definition, Components, Security, Threats, Best practices - Digital payments – Components, stake holders, Modes of digital payments - Banking Cards, Unified Payment Interface (UPI), e-Wallets, Unstructured Supplementary Service Data (USSD), Aadhar enabled payments, Digital payments related common frauds and preventive measures. RBI guidelines on digital payments and customer protection in unauthorised banking transactions. Relevant provisions of Payment Settlement Act,2007.

Digital Devices Security, Tools and Technologies for Cyber Security: End Point device and Mobile phone security, Password policy, Security patch management, Data backup, Downloading and management of third party software, Device security policy, Cyber Security best practices, Significance of host firewall and Ant-virus, Management of host firewall and Anti-virus, Wi-Fi security, Configuration of basic security policy and permissions

Case studies and Assignments:

1. Prepare checklist for following scenarios :
   a) Reporting cybercrime at Cybercrime Police Station.
   b) Reporting cybercrime online.
   c) Using popular social media platforms.
   d) Secure net banking.
2. Demonstrate the following:
   a) Reporting phishing emails, email phishing attack and preventive measures
   b) Reporting and redressal mechanism for violations and misuse of Social media platforms.
3. Manage the following activities:
   a) Privacy and security settings for popular Social media platforms, Mobile Walletsand UPIs.
   b) Application permissions in mobile phone.
4. Perform the following activities:
   a) Setting, configuring and managing three password policy in the computer(BIOS, Administrator and Standard User).
   b) Setting and configuring two factor authentication in the Mobile
5. Demonstrate the following:
   a) Security patch management and updates in computer and mobiles.
   b) Wi-Fi security management in computer and mobile.
6. Install and configure computer Anti-virus & Computer Host Firewall.

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Design appropriate checklists and procedures for secure cyber practices and effective response to cybercrime incidents across various platforms.	Apply
CO2: Illustrate the functioning of cyberspace infrastructure and demonstrate how regulatory frameworks address cyber threats.	Apply
CO3: Analyze privacy and security configurations in social media platforms and digital applications to identify potential risks and propose suitable mitigation strategies.	Analyze
CO4: Apply evolving cybersecurity tools and device protection practices through continuous learning to address emerging digital security challenges.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	3	-	-	2	-	-	2	2	-	-		
CO2	3	-	-	-	-	-	-	-	-	-	-	-		
CO3	-	2	-	-	2	-	-	1	2	2	-	-		
CO4	3	-	-	-	2	-	-	-	-	-	-	2		

High-3; Medium-2;Low-1

Text Book(s):

T1. Cyber Crime Impact in the New Millennium, R. C Mishra. Auther Press. 2010.

T2. Cyber Security Understanding Cyber Crimes, Computer Forensics and Legal Perspectives by Sumit Belapure and Nina Godbole, 1st Edition, Wiley India Pvt. Ltd, 2011.

T3. Security in the Digital Age: Social Media Security Threats and Vulnerabilities by Henry A. Oliver, Create Space Independent Publishing Platform, PearsonEducation, 2001.

Reference Book(s):

R1. Network Security Bible, Eric Cole, Ronald Krutz, James W. Conley, 2nd Edition, Wiley India Pvt. Ltd, 2001

R2. Security Fundamentals of Network by E. Maiwald, McGraw Hill ,2014

R3. Cyber Laws: Intellectual Property & E-Commerce Security by Kumar K,Dominant Publishers, 2011.

Web References:

1. https://unacademy.com/content/upsc/study-material/science-and-technology/initiatives-taken-by-indian-government-for-cyber-security/
2. https://cybercrime.gov.in/
3. https://www.meity.gov.in/cyber-security-division
4. https://intellipaat.com/blog/what-is-cyber-security/

Course Code: 23AUE050		Course Title: Entrepreneurship Development (Common to all Programmes)	
Course Category: Minor		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to develop entrepreneurial mindset and skills by identifying and validating problems through human-centered design, analyzing markets and customers to create value propositions and MVPs, exploring business models with financial and feasibility analysis, and preparing investible pitch decks to attract stakeholders

Module I **22 Hours**

Entrepreneurial Mindset

Introduction to Entrepreneurship: Definition – Types of Entrepreneurs – Emerging Economics – Developing and Understanding an Entrepreneurial Mindset – Importance of Technology Entrepreneurship – Benefits to the Society.

Opportunities

Problems and Opportunities – Ideas and Opportunities – Identifying problems in society – Creation of opportunities – Exploring Market Types – Estimating the Market Size, - Knowing the Customer and Consumer - Customer Segmentation - Identifying niche markets – Customer discovery and validation; Market research techniques, tools for validation of ideas and opportunities

Activity Session: Identify emerging sectors / potential opportunities in existing markets - Customer Interviews: Conduct preliminary interviews with potential customers for Opportunity Validation - Analyse feedback to refine the opportunity.

Prototyping & Iteration

Prototyping – Importance in entrepreneurial process – Types of Prototypes - Different methods – Tools & Techniques. Hands-on sessions on prototyping tools (3D printing, electronics, software), Develop a prototype based on identified opportunities; Receive feedback and iterate on the prototypes.

Module II **23 Hours**

Business models & pitching

Business Model and Types - Lean Approach - 9 block Lean Canvas Model - Riskiest assumptions to Business Models – Using Business Model Canvas as a Tool – Pitching Techniques: Importance of pitching - Types of pitches - crafting a compelling pitch – pitch presentation skills - using storytelling to gain investor/customer attention.

Activity Session: Develop a business model canvas for the prototype; present and receive feedback from peers and mentors - Prepare and practice pitching the business ideas- Participate in a Pitching Competition and present to a panel of judges - receive & reflect feedback

Entrepreneurial Ecosystem

Understanding the Entrepreneurial Ecosystem – Components: Angels, Venture Capitalists, Maker Spaces, Incubators, Accelerators, Investors. Financing models – equity, debt, crowdfunding, etc, Support from the government and corporates. Navigating Ecosystem Support: Searching & Identifying the Right Ecosystem Partner – Leveraging the Ecosystem - Building the right stakeholder network

Activity Session: Arrangement of Guest Speaker Sessions by successful entrepreneurs and entrepreneurial ecosystem leaders (incubation managers; angels; etc), Visit one or two entrepreneurial ecosystem players (Travel and visit a research park or incubator or makerspace or interact with startup founders).

Course Outcomes	**Cognitive Level**
At the end of this course, students will be able to:	
CO1: Apply entrepreneurial mindset principles to identify societal problems and transform them into viable business opportunities.	Apply
CO2: Develop prototypes using suitable tools and techniques for the validated opportunities through iterative processes.	Apply
CO3: Demonstrate a Business Model Canvas using the Lean approach and pitch the startup idea effectively using storytelling and presentation skills.	Apply
CO4: Analyze customer segments, market size, and niche markets to validate entrepreneurial opportunities through market research and customer interviews.	Analyze
CO5: Evaluate the role and components of the entrepreneurial ecosystem to identify and engage the right ecosystem partners and funding models for startup success.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	1	-	-	-	-	-	-	-	-
CO2	-	-	3	-	1	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	1	1	-	-	-	-
CO4	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO5	-	-	-	2	-	-	-	-	-	-	1	1	-	-

High-3; Medium-2;Low-1

Reference Book(s):

T1. Robert D. Hisrich, Michael P. Peters, Dean A. Shepherd, Sabyasachi Sinha Entrepreneurship, McGrawHill, 11th Edition,2020.

T2. Ries, E. The Lean Startup: How Today's Entrepreneurs Use Continuous Innovation to Create Radically Successful Businesses. Crown Business,2011.

T3. Blank, S. G., & Dorf, B. The Startup Owner's Manual: The Step-by-Step Guide for Building a Great Company. K&S Ranch.2012.

T4. Roy, R. Indian Entrepreneurship: Theory and Practice. New Delhi: Oxford University Press,2017.

T5. Osterwalder, A., & Pigneur, Y. Business Model Generation: A Handbook for Visionaries, Game Changers, and Challengers. John Wiley & Sons,2010.

Course Code: 23AUE051		Course Title: Design Thinking and Innovation (Common to all Programmes)	
Course Category: Major		Course Level: Practice	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to equip learners with practical skills in design thinking, empathy, prototyping, testing, and implementation for user-centered innovation and effective product development.

Module I **17+6 Hours**

Introduction- Importance of Design Thinking, Human Centered Design, Six-Step Design Thinking Process-Framework for Innovation-DT-a nonlinear process.

Empathy-importance of empathy in design thinking- empathy vs sympathy- steps of empathize-understanding customer needs-empathy methods and tools-empathy map-5W 1H framework-empathize in UX/UI Design-users Interview

Module II **18+4 Hours**

Prototype: Introduction to Proof of concept-MVP-Prototype and its types-prototype methodology- innovation and its types-Tools for prototyping: concept sketching/CAD/3D Printing.

Testing: Importance of testing in product development-design validation-market analysis: TAM-SAM-SOM-EVG.

Implementation - redesign of solution and iterative process.

List of activities

Core Stream

Empathy

1. What challenges does the user face daily commuting to work place?
2. What are the user's biggest frustrations when interacting with vehicle maintenance engineer?
3. Understand the user for building old age home.

Define

1. A construction site supervisor needs better real-time communication tools because delayed updates cause safety risks. (Provide the empathy data)
2. "Drivers get confused by inconsistent road signs," create: "How might we improve road sign clarity to reduce driver confusion?"
3. A daily commuter needs a safer way to cross busy intersections because current pedestrian signals are confusing and slow. (Provide the empathy data)

Ideate

1. Develop a creativity safer vehicle dashboard design
2. Develop an improved road drainage system
3. Design an innovative solution to reduce urban flooding caused by heavy rains.
4. Design a Hybrid engine designs incorporating solar panels on the car roof.

Prototype

1. Prototype development (both low fidelity and high fidelity) on any real world problem

IT and Circuit Stream:

Activity 1:

Students role-play as designers and users- create an empathy map with 4 quadrants: *Says, Thinks, Does, Feels*

Circuit Stream- Empathy Interview and Persona Creation

Define- development of problem Statement-Elements of a Good Problem Statement-Tools: Point-of-View (POV) Statements-How Might We (HMW) Questions-User Personas.

Ideation in Design Thinking-Importance of Ideation-Metrics of ideation -tools: Brainstorming-Mind Mapping-SWOT.

Activity 2:

IT Stream- SWOT analysis on software project idea.

Circuit Stream -Idea Pitch Canvas using Brainstorming + Mind Mapping

Convert ideas into quick prototypes and validate through early testing.

Activity 3:

IT Stream -Build a simple algorithm to test feasibility- TAM-SAM-SOM market analysis chart

Circuit Stream -MVP Canvas and Concept Sketching

Circuit Stream -Iterative Redesign and Peer Testing Sprint

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply design thinking tools like empathy mapping, problem definition, and ideation to create user-centered innovative solutions.	Apply
CO2: Apply prototyping, innovation, testing, and iterative redesign techniques in product development and market analysis..	Apply
CO3: Apply design thinking to develop, prototype, and validate innovative engineering solutions in capstone projects for real-world applications.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	2	-	-	-	2			2	2	2	2	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Sabell Osann, Lena Mayer , Inga Wiele ,The Design Thinking Quick Start Guide: A 6-Step Process for Generating and Implementing Creative Solutions, Wiley, 2020.

T2. Christian Müller-Roterberg, Handbook of Design Thinking, Kindle Direct Publishing,2018.

Reference Book(s):

R1. Teun den Dekker, Design Thinking, Taylor & Francis, International edition, 2020.

R2. Kaushik Kumar, Divya Zindani, J.Paulo Davim, Design Thinking to Digital Thinking, Springer, 2019.

R3.S. Balaram, Thinking Design, SAGE Publications, 2011.

Course Code: 23ITE047		Course Title: Intellectual Property Rights (Common to all Programmes)	
Course Category: Minor		Course Level: Higher	
L:T:P(Hours/Week) 3:0 :0	Credits:3	Total Contact Hours: 45	Max Marks: 100

Course Objectives:

The course is intended to learn the fundamental concepts of Intellectual Property Law, including patent classifications, trademark strategies, and copyright protections.

Module I **22 Hours**

Intellectual Property: An Introduction: Intellectual Property Law: Patent Law-Copyright Law-Trademark Law- Trade secret Law-Right of Publicity-Paralegal tasks in Intellectual Property Law-Ethical obligations of the paralegal in Intellectual Property Law-Trade secrets: Protectible as a trade secret-Maintaining trade secrets-Protecting an Idea.

Patents: Rights and Limitations: Sources of patent law-Subject matter of Patents: Utility Patents-Plant Patents-Design Patents- Design Patents and copyright-Design Patents and trademarks-Computer Software, Business methods and Patent Protection-Rights under Patent Law-Patent Requirements-Limitations on Patent Rights-Patent Ownership.

Module II ` **23 Hours**

Patents: Research, Applications, Disputes, and International Considerations: Patent Search Process-Patent Application Process-Patent Infringement-Patent Litigation, International Patent laws.

Principles of Trademark: Trademarks and Unfair Competition-Acquiring Trademark Rights-Types of Marks, Strong Marks Versus Weak Marks-Selecting and Evaluating a Trademark-International Trademark Laws.

Principles of Copyrights: Sources of Copyright Law- The Eight Categories of Works of Authorship-Derivative Works and Compilations- Rights and Limitations: Grant of Exclusive Rights–Copyrights Ownership- International Copyright Laws.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1: Apply the fundamental concepts of Intellectual Property Law to real- world scenarios.	Apply
CO2: Demonstrate an understanding of the Rights and Limitations of various patents through practical examples.	Apply
CO3: Analyze the process of patent searching and application filing to assess its effectiveness in protecting intellectual property.	Analyze
CO4: Examine the principles of trademark and copyright to differentiate their roles and implications in intellectual property law.	Analyze

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	2	-
CO2	-	-	-	2	-	-	-	-	-	-	-	-	-	2
CO3	-	3	-	-	2	-	-	-	-	2	-	-	-	-
CO4	-	2	-	-	3	-	-	3	2	-	-	-	-	-

High-3; Medium-2;Low-1

Text Book(s):

T1. Richard Stim, “Intellectual Property: Copyrights, Trademark and Patents”, Cengage learning, 2nd edition 2012.

Reference Book(s):

R1. Deborah E. Bouchoux, “Intellectual Property: The Law of Trademarks, Copyrights, Patents and Trade Secrets”, Cengage Learning, 3rd Edition, 2013.

R2. Prabuddha Ganguli, “Intellectual Property Rights: Unleashing the Knowledge Economy”, McGraw Hill Education, 2017.

R3. David Llewelyn, Tanya Frances Aplin, “Intellectual Property Patents, Copyrights, Trademarks & Allied Rights”, Sweet & Maxwell, 2023.

R4. William F. Patry ,"Principles of Intellectual Property: Patents, Trademarks, and Copyrights", Wolters Kluwer, 2023.

Web References:

1. https://ipindia.gov.in/writereaddata/Portal/ev/sectionsindex.html

OPEN ELECTIVE

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

Course code: 23EVO001		Course Title: Microelectronics	
Course Category: Open Elective		Course level: Higher	
L: T:P(Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objective:
To provide a thorough understanding of semiconductor devices and their operation in analog circuit design and to develop analytical and design skills for building and evaluating electronic amplifiers using BJTs and MOSFETs.

Module I: Semiconductor Devices and Basic Amplifier Concepts 22 Hours

Semiconductor Fundamentals: Energy bands, charge carriers, drift, and diffusion current, p-n junction: I-V characteristics, small-signal model. **Diode Circuits:** Ideal diode model, piecewise-linear model, Rectifiers, clamping and clipping circuits, Zener diode voltage regulators

Bipolar Junction Transistor (BJT): BJT operation modes, characteristic curves, BJT models: DC and small-signal hybrid-π model, Biasing methods: fixed bias, voltage-divider bias, Load line and Q-point stability. **MOSFET Devices:** Structure and operation of enhancement-type NMOS and PMOS, Threshold voltage, I-V characteristics, modes of operation, DC analysis and biasing of MOSFETs

Module II: Amplifier Design and Frequency Response 23 Hours

Basic Amplifier Building Blocks: Concept of amplification, gain, input and output resistance, Small-signal operation and modeling, Common emitter and common source amplifiers. **Multistage Amplifiers:** Coupling methods (RC, direct, transformer) Cascading gain stages and loading effect, Level shifting and bias stabilization in multi-stage circuits.

Frequency Response of Amplifiers: Low-frequency and high-frequency analysis, Bode plots, poles, and zeros. Miller's Theorem and its application, Dominant pole approximation. **Feedback and Stability:** (Introductory) Concept of negative feedback in amplifiers, Effects on gain, input/output resistance, bandwidth, Types of feedback topologies (series-shunt, etc.)

Course Outcomes		Cognitive Level
At the end of this course, students will be able to:		
CO1:	Interpret the characteristics and operation of diodes, BJTs, and MOSFETs using appropriate models.	Apply
CO2:	Design biasing circuits for BJTs and MOSFETs to achieve desired operating points.	Apply
CO3:	Analyze single-stage and multi-stage transistor amplifiers for voltage gain and impedance.	Analyze
CO4:	Determine the frequency response of BJT and MOSFET amplifiers using small-signal equivalent models	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High = 3, Medium = 2, Low = 1

Text Book

T1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, 7th ed., New York, NY, USA: Oxford University Press, 2015.
T2. J. Millman and C. C. Halkias, Electronic Devices and Circuits, 2nd ed., New York, NY, USA: McGraw-Hill, 2008.
T3. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed., Upper Saddle River, NJ, USA: Pearson, 2013.

Reference Books

R1. D. A. Neamen, Microelectronics: Circuit Analysis and Design, 4th ed., New York, NY, USA: McGraw-Hill, 2010
R2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 7th ed., Boston, MA, USA: Pearson, 2014.
R3. M. H. Rashid, Microelectronic Circuits: Analysis and Design, 3rd ed., Boston, MA, USA: Cengage Learning, 2011.
R4. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed., Hoboken, NJ, USA: Wiley, 2009.

Web References

1. https://nptel.ac.in/courses/117102060
2. https://nptel.ac.in/courses/108105132
3. https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/

Course code: 23EVO002		Course Title: Nano Electronics	
Course Category: Open Elective		Course level: Higher	
L: T:P (Hours/Week) 3: 0: 0	Credits:3	Total Contact Hours:45	Max Marks:100

Course Objective:
To introduce the fundamental principles, materials, and device physics at the nanoscale and to develop the ability to analyze and apply nanoscale technologies in modern electronic devices.

Module I: Fundamentals of Nanoscience and Materials **22 Hours**

Introduction to Nanoscience and Nanotechnology: Evolution and scope, Top-down vs bottom-up approaches, Interdisciplinary nature, and applications. Quantum Effects at the Nanoscale. **Nanomaterials and Structures:** Carbon nanostructures: fullerenes, CNTs, graphene, Quantum dots, nanowires, nanorods, nanoshells, Metal and semiconductor nanoparticles

Synthesis Techniques: Physical methods: sputtering, evaporation, Chemical methods: sol-gel, CVD, hydrothermal, Self-assembly, and template-based growth. **Characterization Techniques:** SEM, TEM, AFM, XRD, Importance of scale, resolution, and surface analysis

Module II: Nanoelectronic Devices and Applications **23 Hours**

Nanoelectronic Devices: Device miniaturization and scaling limits, Short-channel effects in MOSFETs, Tunnel FETs, FinFETs, GAAFETs, Single Electron Transistors (SETs), Resonant Tunneling Diodes (RTDs). **Carbon-Based and Molecular Electronics:** CNT-FETs: structure, fabrication, operation, Graphene transistors: bandgap tuning and challenges, Molecular wires, and diodes.
Fabrication Techniques for Nanoscale Devices: Electron-beam lithography, nanoimprint lithography, Bottom-up device assembly techniques. **Applications and Future Trends:** Nano in sensors, memory, energy devices, and healthcare, Challenges in integration, reliability, and scaling, Ethical, safety, and environmental considerations.

Course Outcomes		Cognitive Level
At the end of this course, students will be able to:		
CO1:	Explain quantum effects and the behaviour of materials at the nanoscale.	Apply
CO2:	Identify and classify various nanomaterials and describe their synthesis and characterization.	Apply
CO3:	Analyze the operation of emerging nanoelectronic devices like SETs, CNT-FETs, and FinFETs.	Analyze
CO4:	Apply nanotechnology principles to evaluate device applications and limitations.	Apply

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	-	-	-	-	-	-	-
CO3	-	3	-	-	-	-	-	-	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	-	-	-	-	-	-	-

High = 3, Medium = 2, Low = 1

Text Book

T1. T. Pradeep, Nano: The Essentials – Understanding Nanoscience and Nanotechnology, Tata McGraw-Hill, 2007.

Reference Books

R1. M. Ratner and D. Ratner, Nanotechnology: A Gentle Introduction to the Next Big Idea, Pearson Education, 2003

R2. K. E. Drexler, Engines of Creation: The Coming Era of Nanotechnology, Anchor Books, 1986.

R3. G. Timp (Ed.), Nanotechnology, Springer, 1999.

R4. C. P. Poole and F. J. Owens, Introduction to Nanotechnology, Wiley, 2003.

Web References

1. https://nptel.ac.in/courses/115104124
2. https://nptel.ac.in/courses/117102058
3. https://ocw.mit.edu/courses/6-701-introduction-to-nanoelectronics-spring-2010/

Passed in 5th Board of Studies Meeting held on 09.05.2025
Approved in 20th Academic Council Meeting held on 04.07.2025 BoS Chairman

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